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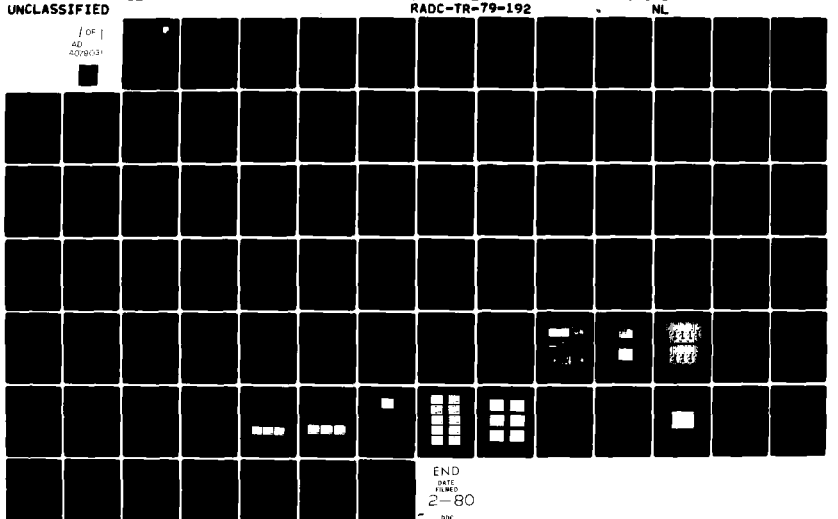

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September 1979

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DESIGN, FABRICATION AND TEST OF A CCD-BASED CORRELATOR/CONVOLVER

Raytheon Company

Arthur M. Cappon
Wolfgang M. Feist
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(9) Interim rept. 26 Sep 77 - 7 Feb 79

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A design has been selected for a CCD-based correlator/convolver having 256 stages of which two analog signals are multiplied. Projected performance goals are 60 dB range, operation up to 10 MHz, 1% relative correlation error, and less than 300 mW power dissipation. The design employs two dual-channel differential CCD's with surface channels, source-follower buffered switched floating gate taps at each stage, four-transistor MOSFET bridge multipliers, and diode injection input. Both by computer simulations, and by a series of test pattern mask measurements in three wafer fabrication phases. (Cont'd)

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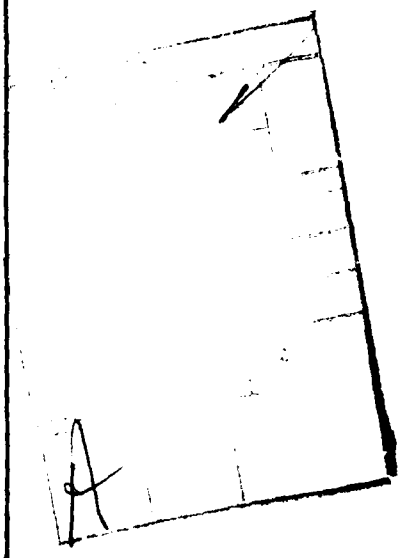
The various elements of the design in isolation and combination were evaluated. The test patterns series included component parts of the full correlator for independent evaluation, transistor multiplier and process characteristic variations, and in addition a complete prototype correlator with 32 stages. The results substantiate the theoretical predicted superiority of the 4-transistor bridge multiplier with dual differential input over previously fabricated multiplier designs due mainly to the cancellation of multiplier distortion terms by virtue of its bridge symmetry. Problems remaining include an error term representing direct feedthrough of the drain input signal, as well as medium-range random variations in transistor parameters larger than desired. These will be addressed in the second half of the contract before design and fabrication of the full 256-stage correlator/convolver.



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SUMMARY

The objective of this contract was to determine the device, circuit, mask, and process design parameters necessary to fabricate a CCD-based correlator/convolver.

Particular emphasis was placed upon the development of an improved (<1 percent error) MOS multiplier since this was known to be a problem in previous designs.

Computer simulations of MOS multiplier configurations led to selection of a design employing differentially driven four-transistor MOS bridge multipliers and floating gate nondestructive taps.

A test pattern integrated circuit was designed, fabricated and tested which verified that the design of the CCDs, MOS multipliers and floating gate tap circuitry probably will meet contract requirements. In addition, a complete 32-stage correlator was fabricated and tested as a test vehicle.

The remainder of the contract will involve the design, fabrication and test of 256-stage correlator/convolver devices. Twenty best effort samples are to be delivered in March 1980.

SECTION I
INTRODUCTION

The purpose of this program is the development of a CCD-based correlator/convolver suitable for use in advanced USAF military electronic systems.

The specific objective of this program is to fabricate and deliver 20 best-effort samples of CCD-based correlator/convolver devices aimed at the design goals listed below in Table 1.

TABLE 1. OVERALL PERFORMANCE GOALS

CCD Dynamic Range	60 dB 70 dB after input normalization
CCD Clock Rate	32 kHz to 10 MHz at 25°C 500 kHz to 10 MHz at +85°C
CCD Size	256 Stages
Relative correlation error (percent of theoretical for pulse waveforms/W 25 percent duty cycle)	1 Percent
Power Dissipation	≤300 mW

The performance goals outlined above were selected to meet or exceed contract requirements.

This (interim) report describes work either completed, in process, or planned under the contract. It begins with a discussion and analysis of design tradeoffs and follows with a description of the process design and mask design used for the first-generation test mask series. Later, test results will be reviewed and plans for the second phase of the program will be described.

SECTION II
TECHNICAL DISCUSSION

2.1 General

The first part of this section contains a brief statement of the problem which includes a definition of correlation and convolution and a presentation of their implementation in block diagram form. This block diagram is based on a design using charge-coupled analog shift registers and MOS analog multipliers. A discussion of the principal problem areas in each circuit implementation is provided.

The second part presents a range of alternative designs which were considered for each part of the device - the CCD, the nondestructive parallel readouts, the multipliers, and the summing amplifier. The discussion will include the relative merits and difficulties of each approach.

Part 3 will present the configuration which was selected for use. Table 2 outlines the design features of the new device.

TABLE 2. CCD-BASED CORRELATOR/CONVOLVER DESIGN FEATURES

CCD		
Surface type	-	For low distortion, low dark current and maximum tap output levels
Two-phase clock but with all four clock busses brought out for reference	-	For minimum complexity combined with ability to reverse direction of reference CCD electronically for convolver operation
Differential operation	-	Permits use of superior multiplier designs, improved dark current and harmonic rejection
Resettable floating gate taps	-	For nondestructive readout
Diode injection input	-	To obtain matched CCD input and output characteristics
Multiplier		
Four MOSFET with source follower buffered inputs	-	For maximum accuracy and minimum errors generated by nonlinearities, offset variations and CCD dark currents

2.2 General Statement of the Problem

The mathematical definition of the correlation C of two real functions f and g defined over the interval $-\infty$ to $+\infty$ is given by Equation (1) below:

$$C(y) = \int_{-\infty}^{\infty} dx\, f(x)\, g(x + y) \qquad (1)$$

One can envision this operation as indicated pictorially in Figure 1. The two functions f and g are aligned next to each other with their axes running in the same direction with the origin of g shifted a distance y. The two displaced functions are multiplied at their adjacent points, and the products are summed. The function C(y) unfolds with increasing y as g moves by f.

The discrete version of Equation (1) for functions defined at equally spaced points is given by Equation (2a).

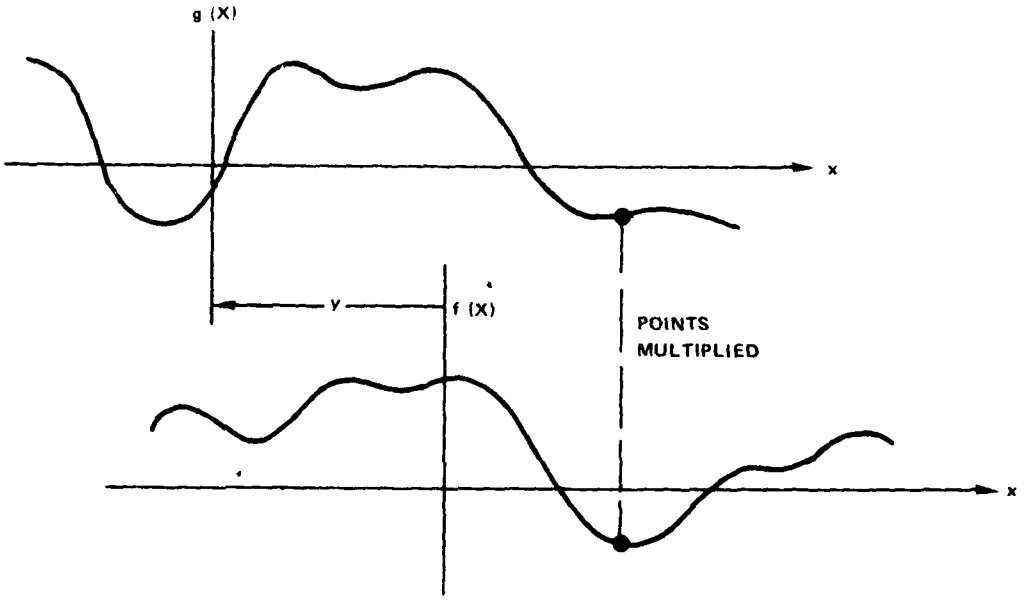


Figure 1. Pictorial Representation of the Correlation Operation

$$C_j = \sum_{i=-\infty}^{+\infty} F_i G_{i+j} \tag{2a}$$

This may reduce further to a finite version if one of the signals for example F, is of finite length. The equation then becomes:

$$C_j = \sum_{i=1}^{N} F_i G_{i+j} \tag{2b}$$

The convolution function C' of two functions f and g is defined by Equation (3).

$$C'(y) = \int_{-\infty}^{\infty} dx\, f(x)\, g(y - x) \tag{3}$$

$$= \int_{-\infty}^{\infty} dx\, f(-x)\, g(x + y)$$

The convolution can be envisioned pictorially as shown in Figure 2. The difference is that one of the functions has the direction of its x-axis reversed. The function g moves by a backward f while the sum of products is being computed.

The discrete and finite versions of the convolution are given by Equations (3a) and (3b).

$$C'j = \sum_{i=-\infty}^{\infty} F_{-i} G_{i+j} \tag{3a}$$

$$C'j = \sum_{i=1}^{N} F_{-i} G_{i+j} \tag{3b}$$

Figure 3 shows a block diagram of the realization of the finite discrete versions of the correlation and convolution.

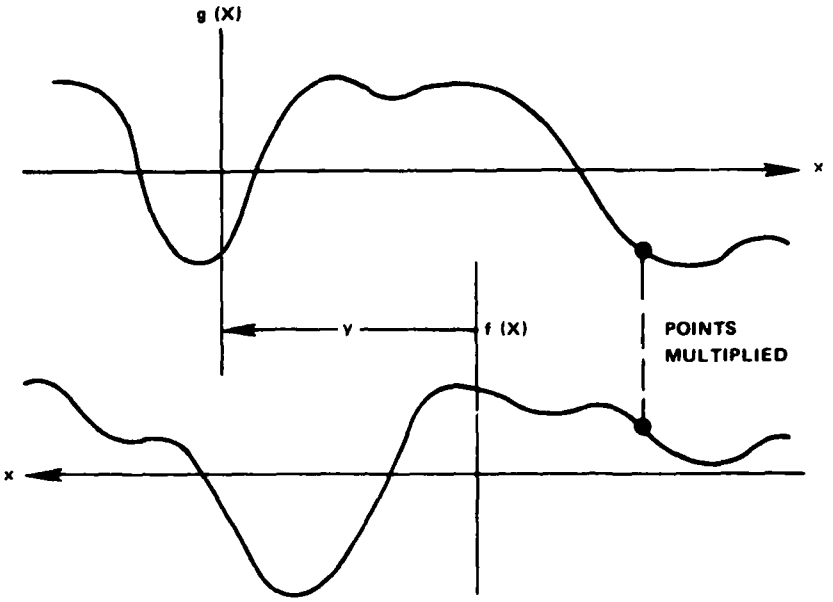


Figure 2. Pictorial Representation of the Convolution Operation

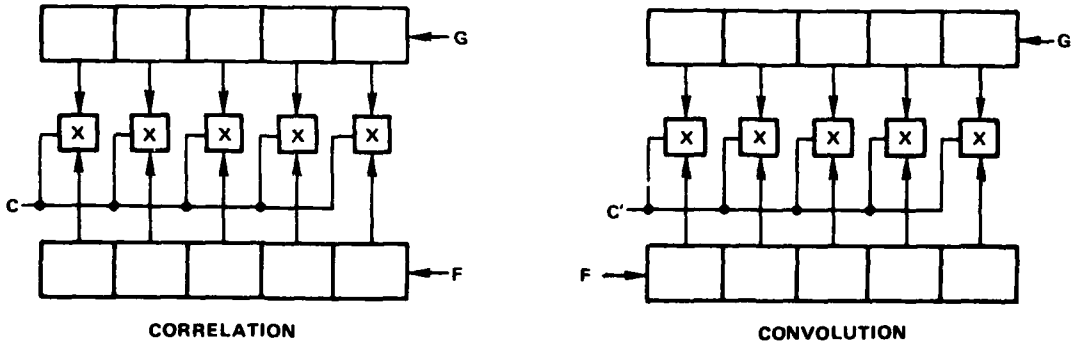


Figure 3. Physical Realization of Correlation and Convolution

The upper and lower registers represent analog shift registers carrying sampled analog data. These could be charge-coupled shift registers with nondestructive parallel readouts. The adjacent signal samples are multiplied by an array of analog multipliers, the outputs of which are summed, for example, on a current bus for multipliers with a current output. The correlation and convolution functions are generated by shifting the samples of G through the upper shift register and carrying out the sum-of-products operation after each shift.

Note that the convolver differs from the correlator only in the direction in which signal F is shifted into the lower shift register. If a single device is desired which is capable of performing both functions, one can readily design a CCD with symmetrical input and sink structures, which, with appropriate clocking, could be made to operate in either direction. This cannot be achieved, however, using two-phase CCDs in which the directionality is determined physically and not electrically. This point will be discussed in greater detail in Subsection 2.4.1.

2.3 Critical Implementation Factors

In constructing an integrated circuit correlator/convolver from CCDs and analog multipliers, each element has critical factors which must be controlled in order to achieve satisfactory performance levels from the complete device. All parts must achieve sufficiently low levels of random noise, have adequate temperature insensitivity, and consume minimum power.

The special considerations that apply to the various elements are set forth below.

2.3.1 Charge-Coupled Shift Register

Linearity

The CCD, considered here to include the nondestructive parallel outputs, must achieve an adequate level of input-to-output linearity. The individual conversions between voltages and charge at the input and outputs need not be linear. Indeed, as discussed in more detail later, floating gate outputs are inherently nonlinear, and generally must be used with CCD input techniques with a corresponding nonlinearity.

Variations

Since the CCD has a single input structure, one source of variation from cell-to-cell is eliminated. Variation of output tap sensitivity is a factor to be considered.

Fixed Pattern Noise

In addition to contributing to the random noise level, thermal carrier generation (dark current) introduces nonrandom variations into the signal charge. For example, if signal F in Figure 3 is loaded into the lower CCD shift register and then held there as a signal G is swept by it, dark current will steadily accumulate. This will cause signal F to acquire a dc offset and, to the extent that dark current is nonuniform, an ac variation from cell-to-cell. Similarly, a signal G clocked through the CCD at a slow steady rate will acquire an approximately linear ramp offset due to the greater accumulation of dark current in cells containing signal which has been in the CCD longer. Dark current and its uniformity are, therefore, important considerations in the CCD.

Transfer Efficiency

As signals are shifted through a CCD, a small fraction of each signal packet is left behind and becomes a part of the next signal packet. This gives rise to a bandwidth change and phase shift in the signal.

2.3.2 Analog Multipliers

Linearity/Accuracy

The linearity and accuracy of the multiplier are critical characteristics. Depending on the types of functions being correlated, certain error terms are far more critical than others. In a computer simulation of the matched filtering of an FM chirp waveform, a 10 percent term of the form $fg^2 + gf^2$ raised the sidelobes only to -32 dB. A mere 1 percent term of the form $f^2 + g^2$ caused a slightly greater degradation in sidelobe level.

Variation

Even if each individual multiplier in the IC had perfect linearity, variation in gain could be a source of trouble.

2.3.3 Summing Amplifier

Nearly any scheme for adding bipolar numbers in the form of currents will involve the use of bias currents that must be balanced out. Consequently, common-mode rejection will be a critical factor in the summing amplifier.

2.4 Options

This section presents a catalog of the major options available for the elements of the integrated circuit correlator/convolver.

2.4.1 CCD Design

Channel Type

The CCD may be of either the surface channel or the buried channel type. The buried-channel CCD (BCCD) offers superior charge transfer efficiency and maximum operating speed. In theory, it offers a superior signal-to-noise ratio, but in practice this is offset by the low output signal levels, especially from a floating gate detector. The surface channel CCD (SCCD) is somewhat simpler to fabricate, exhibits lower dark current, carries more charge, and is intrinsically more linear.

Clocking Technique

CCDs are commonly made with 2-phase, 3-phase, or 4-phase clocking structures. All can be operated with one electrode held at a dc level instead of being clocked. These modes of operation are named 1-1/2 phase, 2-1/2 phase, and so on. The 3-phase structure provides the minimum cell pitch. Its fabrication, however, requires either three gate layers or the cross-connection of gates fabricated in two layers. The addition of a fourth gate per cell permits the gates to be made in two interdigitated layers with

no cross-connections. This 4-phase structure, if operated with overlapping clocks, can store charge under at least two gates at all times. This gives the 4-phase CCD the greatest charge handling capacity. The 2-phase structure can be considered a degenerate form of the 4-phase structure with neighboring gates connected in pairs and directionality of transfer built in physically, for example, by changing the oxide thickness or by changing the substrate doping density by ion implantation. The 2-phase structure has the advantage of requiring the fewest number of clocks and clock distribution buses. The half-phase versions all offer a reduction in clock number compared to the corresponding whole-phase design, but a significant penalty in dynamic range results unless the voltage swing of the remaining clocks is increased.

Finally, one should note that all of the clock schemes except 2-phase and, 1-1/2-phase are capable of shifting charge in either direction. For example, exchanging the signals on clock phases 2 and 3 of a 3-phase device or 2 and 4 of a 4-phase device will reverse the direction of transfer. A 2-phase device in which all four clock lines are accessible can have its gates connected for bidirectional operation. This involves the structural complexity of a 4-phase device but the clock requirements of a 2-phase device. This is illustrated schematically in Figure 4. The switch can be implemented by discretionary bonding or with FET switches.

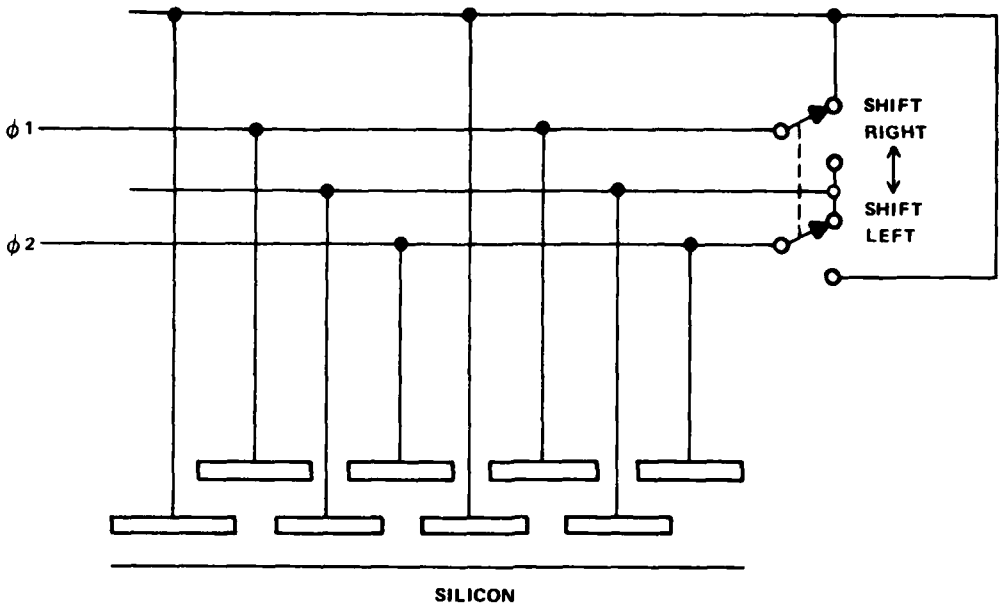


Figure 4. Method for Making 2-Phase Devices Bidirectional

Input Structure

Two generally used input techniques for CCDs are called charge equilibration and gated diode. In the former, as shown in Figure 5(A), a metering input well is formed as a result of the difference between the voltages on IG1 and IG2. A pulse applied to the input diffusion overfills the input region. The excess charge then flows back to the diffusion until equilibrium is established. This input technique results in a very linear conversion of the input voltages on IG1 and/or IG2 to charge (less than 0.1 percent error is possible); normal and inverting inputs are available; and the noise level is very low. For most purposes this is the preferred input technique.

The gated diode input is illustrated in Figure 5(B). Here the signal is connected to the input diffusion. When IG1 is pulsed on, the input well under IG2 is filled to a channel potential equal to the input signal level. The conversion of voltage to charge is not linear because of the variable depletion capacitance, but floating gate detectors, as discussed below, sense not the signal charge but the surface potential. The gated diode input thus tends to match the floating gate output for an overall linear transfer function.

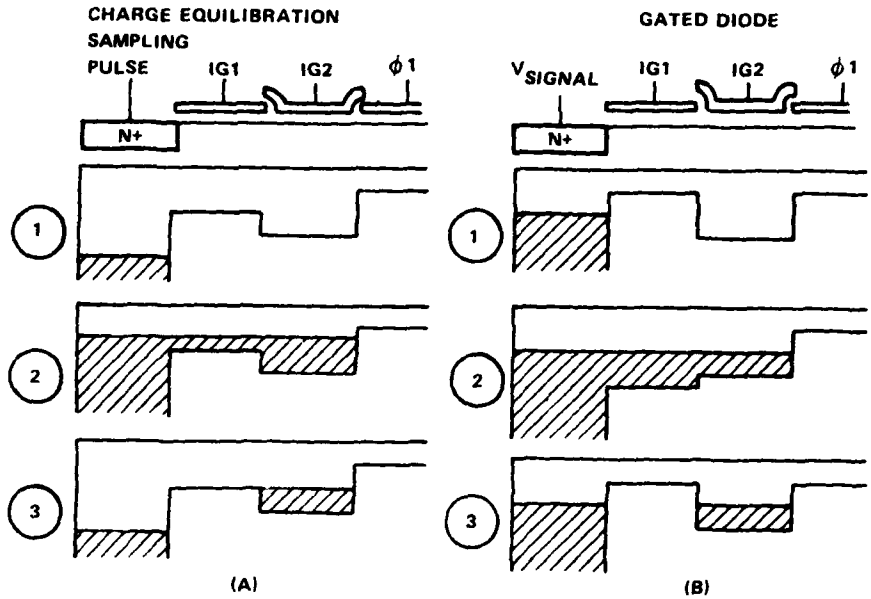


Figure 5. Charge Equilibriation and Gated Diode CCD Input Techniques

Nondestructive Parallel Readout

The correlator design requires CCDs with outputs at every tap, and the output sensing must be performed in a nondestructive way with a minimum of degradation. Two general types of nondestructive readout are available. One is called the floating diffusion technique. Here the charge is made to flow onto a diffusion, which may be under one of the gates of the CCD. The diffusion acts as a conductor which comes to the potential of the channel and can be connected to a MOSFET gate for sensing. Since the diffusion is floating (not connected to any charge source outside the CCD), total charge is conserved and the signal in the CCD passes on unchanged as the clocks cycle. The diffusion is loaded down, however, by the sensing circuitry, and there can be a problem of uneven charge redistribution under the gate. More serious yet is a substantial degradation of charge transfer efficiency due to the formation of a structure that is acting essentially as a bucket brigade device. This problem has been encountered in CCD shift register designs with diffused corners. The problem is acceptable in some

cases because of the small number of corners; however a floating diffusion sensor at each stage of the CCD would probably not be acceptable in most cases. The transfer problem is substantially reduced when half-phase clocking is used with dc on the gate over the floating diffusion.

The floating diffusion does have the advantage of tending to sense charge in the channel, especially when the circuit loading on the diffusion becomes large. In that case, the diffusion voltage does not change very much, and thus the depletion capacitance remains nearly constant.

The other nondestructive readout technique is the floating gate (FG). Numerous realizations are possible, but they fall generally into two classes depending on how the floating gate is made to reach the necessary dc bias level. In one case, the FG is simply connected through an FET switch to the appropriate clock line. Just before the signal charge arrives under the FG, this switch is opened allowing the gate to float.

This technique sometimes requires a change from the normal clocking technique. For example, with normal 4-phase overlapping clocks, the signal charge enters the region under any gate as soon as the gate goes ON. This cannot be permitted to occur with the switched FG. The clocking must be modified as shown in Figure 6 so that the two gates adjacent to the floating gate are OFF until after the float switch opens. The maximum charge handling capacity is reduced to one half.

The 3-phase structure cannot be operated in this mode because the floating gate must be isolated by OFF gates on both sides while another gate holds the signal charge. Thus, four gates are required. The 2-phase structure with 'push' clocks is a natural for this FG technique because the charge transfers when the clocks make their OFF transitions. The corresponding timing and charge motion diagrams are shown in Figure 7.

The advantages of switched floating gate sensors are follows:

- With this floating gate technique, all of the signal charge is under the FG, and uneven distribution problems do not arise.
- The FG is physically just a regular CCD gate, differing only in the way it is connected. This simplifies fabrication and tends to insure undegraded CCD performance.
- The parasitic loading on the FG can be kept low, increasing its sensitivity.

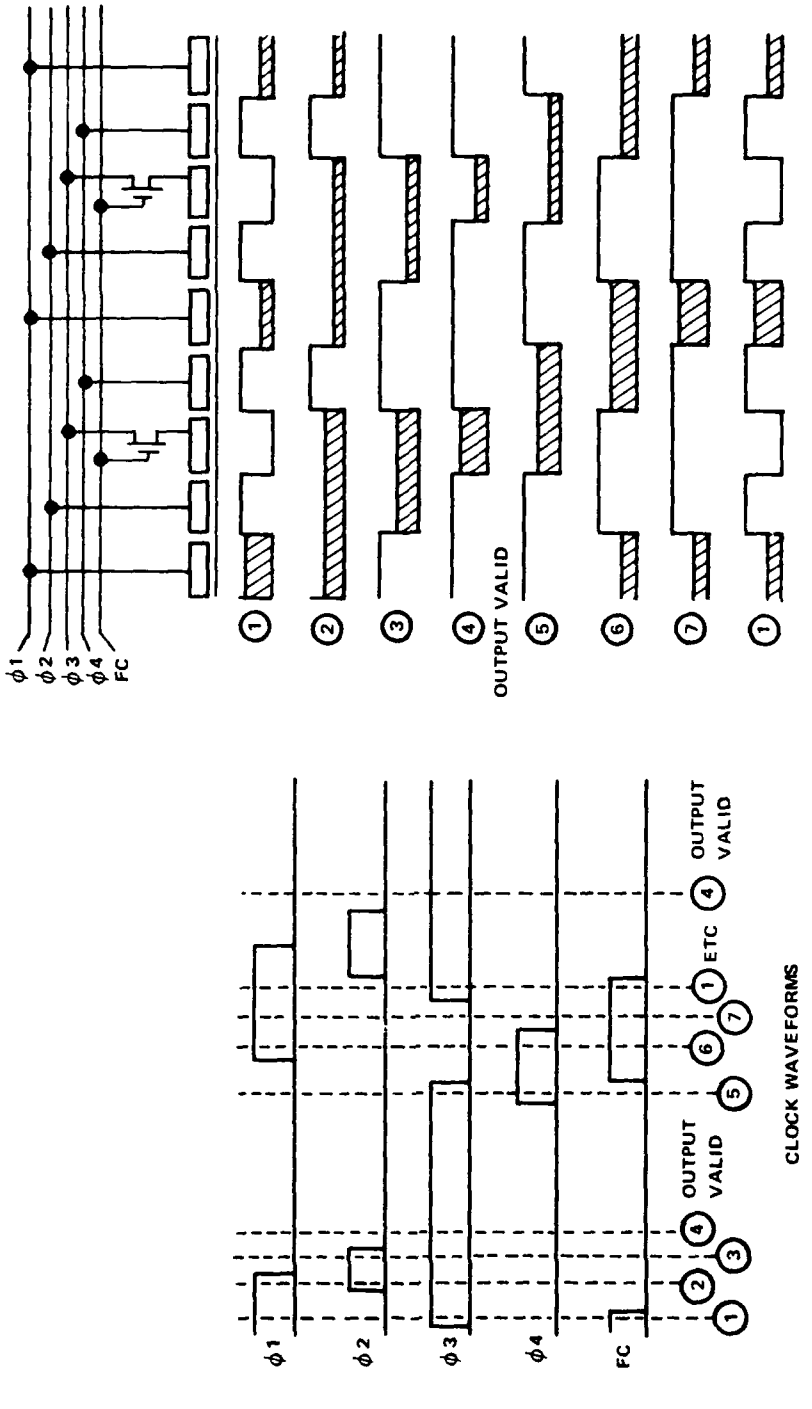


Figure 6. Modification of 4-Phase Clocking Required with Switched Floating Gate Sensors

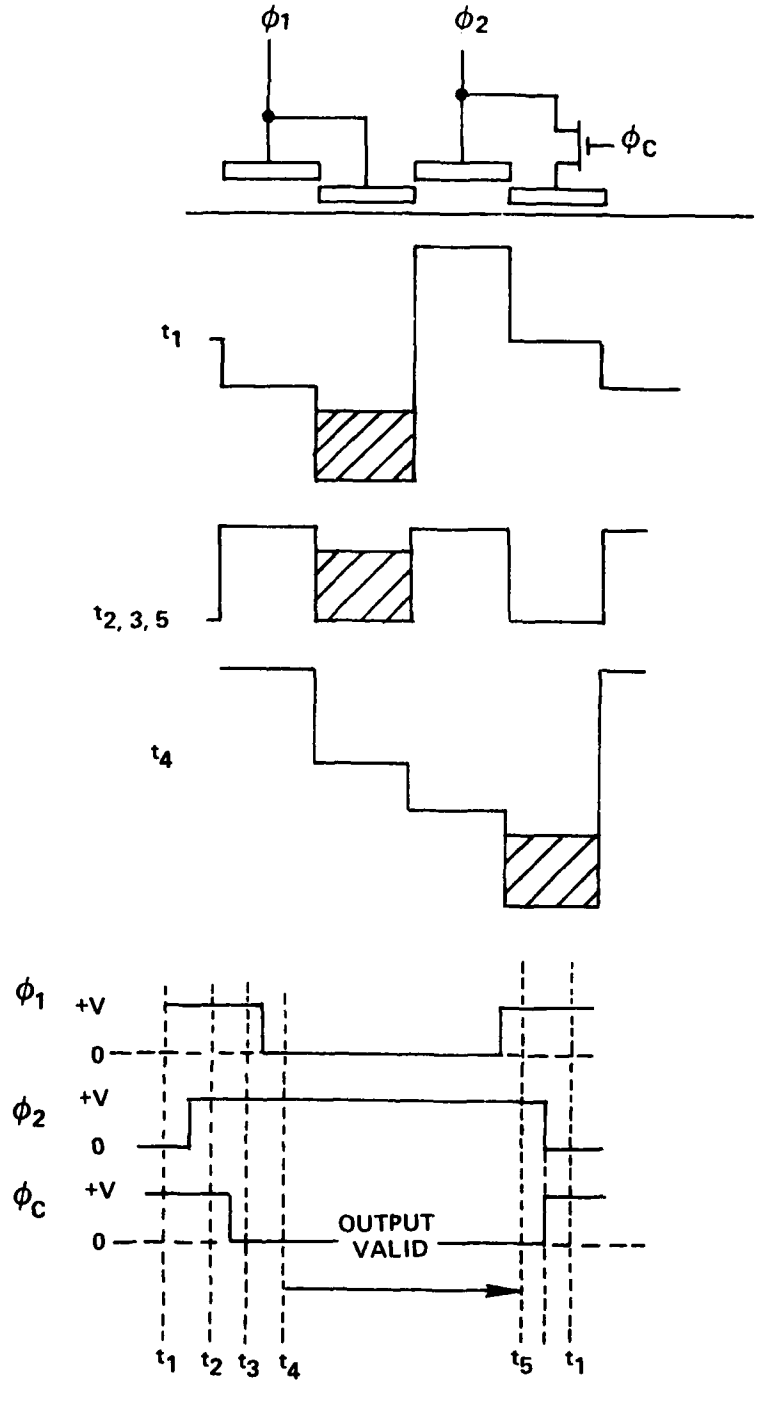


Figure 7. Clock Waveforms and Charge Flow for 2-Phase Clock Operation With Switched Floating Gate Tap

The second type of floating gate is the capacitively coupled floating gate. As with the switched FG, the gate is connected via a FET switch to a clock or reset line. This insures that the desired total charge is present on the gate. The resetting operation need not be carried out very frequently or rapidly and may, therefore, be carried out using a smaller transistor. The clock swing is induced on the FG by means of coupling capacitance between a clock line and the floating gate. There are conflicting considerations concerning this capacitance. If it is very large, the clock signal is coupled in very efficiently, but the FG is heavily loaded down and becomes less sensitive. On the other hand, if the coupling capacitance is small, a much higher amplitude clock is needed. These problems are eliminated when a half-phase clocking scheme is used with the FG serving as the dc gate. In this case the gate is acting more as a switched floating gate.

The capacitively coupled FG has the advantage of being able to work with any clocking technique. It suffers from several disadvantages, however. It can be expected to exhibit greater loading and lower sensitivity; it requires a more elaborate CCD structure with both capacitive and FET connections; and in some implementations it suffers from linearity problems from uneven signal charge distribution under the gates.

2.4.2 Multiplier Designs

Although much work has been done on multipliers in the past, most of it is not applicable to this program since it has emphasized bipolar technology and has been aimed primarily at the analog computer market. The operating principles used in such multipliers have included the following categories:

Bipolar Transconductance Multipliers
Bipolar Carrier Domain Multipliers
Log-Antilog Multipliers
Pulse Modulation Multipliers
Servomechanism Multipliers

Although the previous categories can be used to make very accurate and satisfactory multipliers, the emergence of MOSFET multipliers has rendered them obsolete as far as this program is concerned. Thus, this section will be limited to a discussion of MOS structures only.

Basic MOS Operation

The gate-voltage-controlled drain-to-source conductance of a MOSFET operating in the triode region provides an excellent basis on which to build an analog multiplier. The theoretical relation between the current flowing from drain to source (I_{DS}) and the voltages on the drain and gate relative to the source (V_{DS}, V_{GS}) is given by Equation (4) to terms quadratic in the voltages.

$$I_{DS} = g\, V_{DS} (V_{GS} - V_T - 1/2\, V_{DS}) \tag{4}$$

If the source is not connected to the substrate, the threshold voltage V_T will depend on the source-to-substrate voltage, V_S, an effect sometimes called the back-gate-bias effect. The V_{DS} term inside the parentheses represents an effective shift in threshold due to the back-gate bias effect resulting from the change in average channel potential from drain to source of $1/2\ V_{DS}$. For the sake of accuracy, it should be noted that theoretically this factor is actually slightly greater than 1/2 because the back-gate bias coefficient dV_T/dV_S is greater than unity.

It is assumed that a multiplier will be constructed based on Equation (4) by holding a current bus connected to the source at a fixed potential and measuring the current. Since V_{GS} must be greater than V_T to get any current to flow, the multiplier will only work for one sign of V_{GS}. Since V_{DS} can be either positive or negative, a two quadrant multiplier results.

There are several major problems that must be overcome before the MOSFET can be used as an analog multiplier in an IC correlator. First, since V_D, the drain voltage is to be supplied from a buffered floating gate or floating diffusion sensor, it will consist of a bipolar signal riding on a substantial offset. This will induce an undesirable linear term in the current proportional to V_{GS}. This term can be eliminated by biasing the source to the offset level of the drain voltage. Second, if V_G also comes from a floating diffusion or floating gate sensor, it also will consist of a bipolar signal riding on a dc offset. This will induce an undesirable linear term in the current proportional to V_{DS}. This term could be eliminated by using a differential current bus and bleeding a current proportional to V_{DS} through a resistor corresponding to the FET conductivity with V_{GS} at its dc offset level. The third problem is the large quadratic term in V_{DS}^2. This represents a significant error term in the multiplication.

Solutions to all of these drawbacks of the simple MOSFET multiplier can be better achieved by arranging MOSFETs symmetrically in various ways. Four such arrangements are worthy of serious consideration.

Dual MOSFET Gate-Reference-Balanced Multiplier

In this multiplier, two MOSFETs are connected as shown in Figure 8. The two signals from buffered outputs of the two CCDs are represented by V_D and V_G. A reference voltage $V_G^{(0)}$, equal to the value of V_G when the CCD contains a zero signal, is applied to the balancing MOFSET. The sources of the two transistors are connected to two current buses, which must be held as virtual voltage modes. The output signal is represented by the difference between the currents in the two buses. These buses must be held not as virtual grounds, but rather, as remarked above, at a voltage equal to $V_D^{(0)}$, the value of V_D when the CCD contains a zero signal.

The advantage of this circuit is that it removes all three flaws of the single MOSFET, including the large quadratic term in V_{DS}^2. That term results in equal currents on the two buses and cancels out when the currents are subtracted.

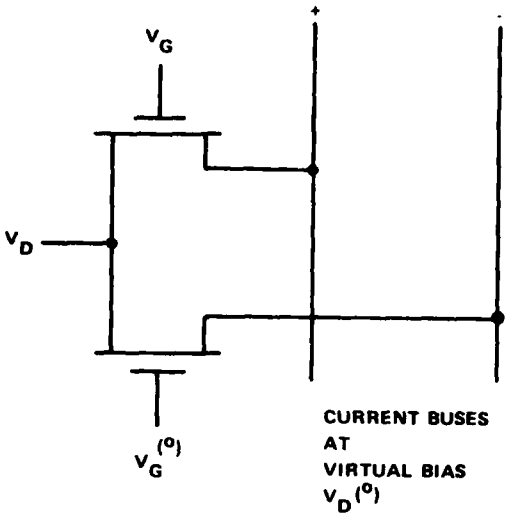


Figure 8. Dual MOSFET Multiplier Structure

Major deficiencies remain nevertheless. Variations in the values of $V_D^{(0)}$ and $V_G^{(0)}$ due to variations in component parameters, CCD bias charge levels, and dark current accumulation will upset the balance in the circuit.

Dual MOSFET Differential-Gate Multiplier

This multiplier is a simple extension of the previous concept and uses the same circuit arrangement. The difference is that the CCD providing the output voltage V_G is configured as a split-channel differential CCD with outputs of $V_G^{(1)} = V_G^{(0)} + V_G^{(S)}$ and $V_G^{(0)} - V_G^{(S)}$, where $V_G^{(S)}$ represents the signal. $V_G^{(1)}$ is applied as V_G in Figure 8; $V_G^{(2)}$ replaces $V_G^{(0)}$ on the other gate. The sensitivity of the multiplier to $V_G^{(0)}$ is eliminated. Moreover, even order nonlinearities in the CCD output signal applied to the gates are also cancelled by the differential arrangement.

Quad MOSFET Dual Reference-Balanced Multiplier

Another improvement over the circuit in Figure 8 is shown in Figure 9. Here the signal applied to the drain is also balanced against a reference. The primary advantage of this circuit is that it relieves the requirement that the current buses be held at $V_D^{(0)}$. It is conceivable that individual $V_D^{(0)}$ references for each cell could be derived in a way that would compensate for cell-to-cell variations.

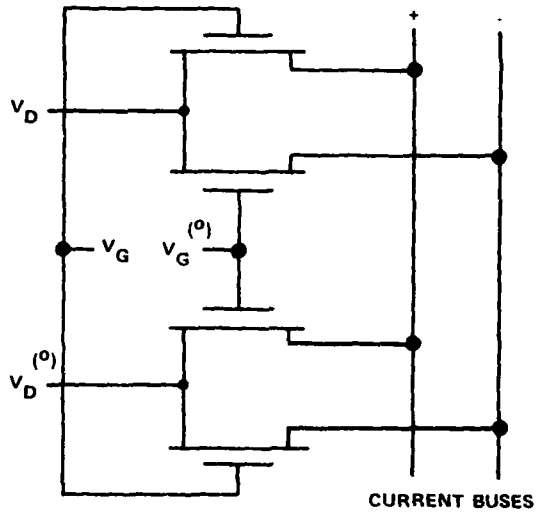


Figure 9. Quad MOSFET Multiplier Structure

Quad MOSFET Dual-Differential Multiplier

This multiplier follows from Figure 9 in the same way that Multiplier No. 2 followed from Figure 8. Both CCD shift registers are now configured as differential CCDs and the reference values $V_G^{(0)}$ and $V_D^{(0)}$ are taken from the CCD channels carrying the inverted signals. The result is a configuration which responds to the two signals to be convolved or correlated only as the product of f.g through terms of cubic order in the signals. Constant terms, terms linear in f or g, terms of the form f^2 and g^2, and all

terms cubic in combinations of f and g are cancelled by symmetry. This is true regardless of distortion in the CCDs and imperfections in the MOSFETs, provided the four MOSFETs in a given multiplier and the two halves of each split-channel CCD are identical.

This circuit configuration is a fundamental multiplier as a result of circuit symmetry and will act as a multiplier to first order when virtually any three terminal device is used. The fact that a single MOSFET is a fairly good multiplier to start with makes the performance that much better. Table 3 shows the terms through 4th order in a general mathematical expansion of the source current as a function of drain and gate voltages, the origin and relative magnitude of the major terms, and which terms are present for the four multiplier designs discussed above.

In the full correlator design, the signals represented by charge in the CCDs appear at the outputs riding on a dc bias. For example, the drain voltage is $V_D = V_D^{(0)} + V_D^{(S)}$. Consequently, a term of the form V_D^2 in Table 3 contributes a constant term, a linear term, and a quadratic term in the signal voltages. Because the dc levels are large, these terms are all first order. A quadratic distortion in the CCD output adds further lower order terms. Table 4 shows the terms that result from the dc offsets and quadratic CCD distortions. The crosses represent first order terms and the dots second order terms.

If the source voltage is balanced to the drain inputs for the multiplier of type one, it has the characteristics of the dual-reference balanced design No. 3. Only the dual-differential design No. 4 cancels all undesired MOSFET multiplier and CCD output amplifier terms to first and second order.

TABLE 3. CHART OF TERMS PRESENT IN FOUR POSSIBLE MULTIPLIER DESIGNS

Form of Term	Source of Term	Relative Magnitude	Dual MOSFET		Quad MOSFET	
			Ref. -Balanced	Differential	Ref. -Balanced	Dual Differential
1	Threshold voltage	Large				
V_G	Gate leakage	Very small	X	X		
V_D	Source drain leakage	Small				
V_G^2			X			
$V_G V_D$	Transconductance - Desired term	Large	X	X	X	X
V_D^2	Drain-voltage induced V_T shift	Large				
V_G^3			X	X		
$V_G^2 V_D$	Mobility decrease at high surface charge	Moderate	X		X	
$V_G V_D^2$	Mobility decrease at surface charge	Moderate	X	X	X	
V_D^3						
V_G^4			X			
$V_G^3 V_D$			X	X	X	X
$V_G^2 V_D^2$			X		X	
$V_G V_D^3$			X	X	X	X
V_D^4			X	X	X	X

TABLE 4. FIRST AND SECOND ORDER ERROR TERMS RESULTING FROM DC OFFSETS AND QUADRATIC CCD DISTORTION

		Resulting Term									
Source Term		1	V_G	V_D	V_G^2	V_GV_D	V_D^2	V_G^3	$V_G^2V_D$	$V_GV_D^2$	V_D^3
First Order	V_GV_D	X	X	X	•	X	•		•	•	
	V_D^2	X		X			X				•
Second Order	$V_G^2V_D$	•	•	•	•	•			•		
	$V_GV_D^2$	•	•	•		•	•			•	
Net Term		X	X	X		•	X		•	•	•

SECTION III
SELECTED DESIGN

3.1 General

The design selected for the correlator/convolver employs two dual-channel differential CCD's with surface channels, source-follower-buffered switched floating gate taps at each stage, and four-transistor MOSFET multipliers. Although this approach requires the greatest chip area, the potential accuracy improvement from the use of four-transistor multipliers in the presence of expected parameter variations (ΔV_T, Δg_m, $\Delta R_{interconnect}$) was found to be well worth the cost in chip area.

Surface channel CCD's were selected because their linearity and dark current characteristics have been superior to those obtainable from buried channel devices. The charge transfer efficiency of surface channel CCD's, especially with the wide channels used here, has been shown to be adequate. This choice *is not* irrevocable, since the same mask set can be used to make a buried channel version.

Two input control gates were provided to each CCD channel so that they can be operated in either the gated diode or potential equilibration mode.

Switched floating gate taps were chosen to ensure that no loss of transfer efficiency would result from the presence of the taps on the delay line.

Source followers were provided to isolate the floating gate taps from the multipliers and the interconnect lines. This improves the sensitivity of the taps, maintains equality of sensitivity for the four CCD channels, eliminates spurious cross-coupling of clock signals due to interconnect capacitance (except for switching transients), and provides the needed current source/sink capability for the taps driving the MOSFET source inputs to the multipliers.

The existing test pattern mask series includes all of the component parts of the full correlator in configurations that allow their independent evaluation. It also includes transistor and process characterization patterns. And, finally, it includes a complete prototype correlator with 32 stages.

The layout rules for the test mask series were changed after a first attempt to design the correlator using the existing (7.5μm) process geometries. Finer line widths and spaces (3.75 μm) were found to lead to great improvements in correlator accuracy as well as reduced silicon area.

The existing Raytheon wafer fabrication process was adopted to the new denser layout rules by making simple adjustments to processing parameters such as exposure times. In addition, a coplanar oxide isolation version of the process was developed which should provide improved yields for the new, denser structure dimensions.

The above design features will be discussed in greater detail in the sections which follow.

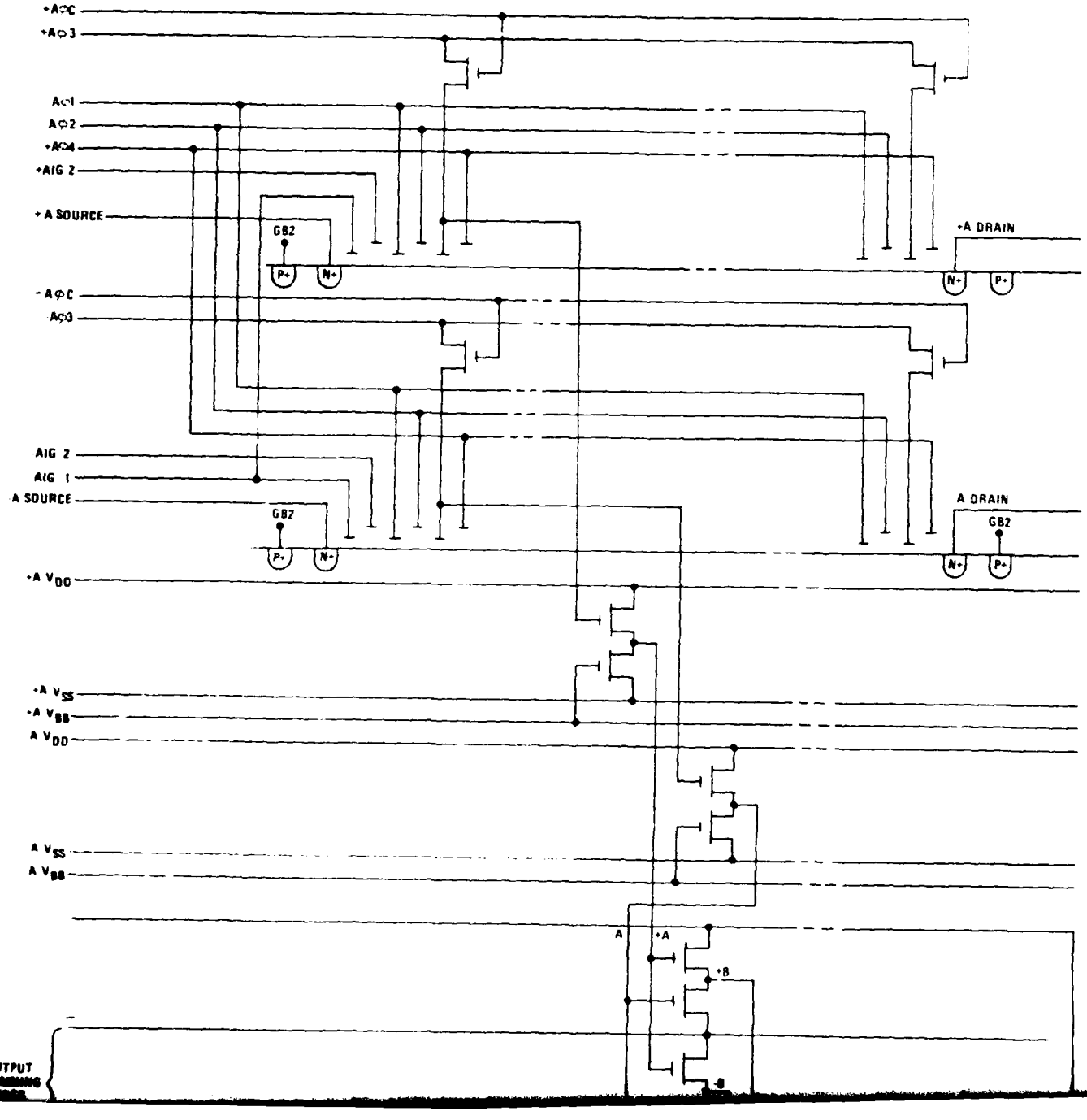
3.2 Device Design

3.2.1 General

Figure 10 shows the schematic of the correlator/convolver with the first stage drawn in detail to show how the differential CCDs are connected to the four transistor multipliers.

The geometries of the circuit components and interconnects were constrained by the necessity to fit all components within the 30 μm pitch of the CCD. A greater CCD pitch could have been used, but this would have resulted in a reduced transfer efficiency.

The second constraint on the circuit components was power dissipation. The 300 mW design goal chosen for this parameter is typical for MOS LSI devices and, with proper heat sinking, should not cause excessive loss of storage time.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+AΦ3
AΦ1
AΦ2
+AΦ4
+AIG 2
+A SOURCE
GB2
P+
N+
+A DRAIN
N+
P+
-AΦC
AΦ3
AIG 2
AIG 1
A SOURCE
GB2
P+
N+
A DRAIN
GB2
N+
P+
+A V_{DD}
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+A
+B
-B
OUTPUT
SUMMING

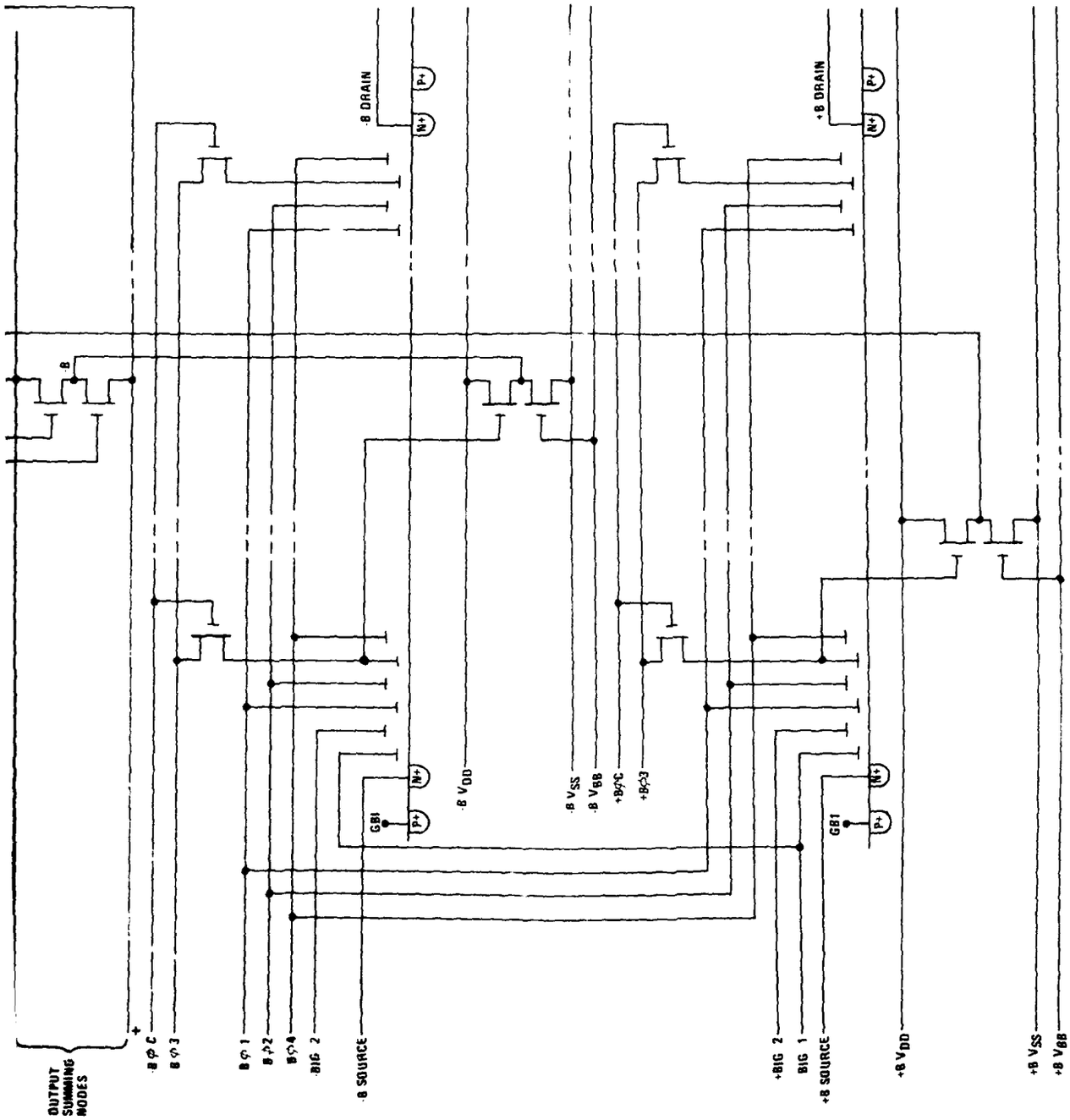


Figure 10. Schematic Diagram (1 Stage) of CCD Correlator/Convolver

Since the main objective of the program was to provide high-performance correlation or convolution (within 1 percent of theoretical), the device design was carried out with chip area and complexity as a secondary consideration.

Computer simulations of the correlator/convolver circuit design were carried out in parallel with mask design since geometric constraints could not be ignored in the optimization process.

The first mask designs used the existing Raytheon process layout rules which featured 7.5 μm line widths and spacings. A more advanced process with smaller features was found to offer such a great advantage in meeting the required accuracy that new layout rules were devised and adopted for this program allowing 3.75 μm line widths and spacings. Only the final designs using the revised layout rules will be described in the pages which follow.

3.2.2 Circuit Design and Optimization

3.2.2.1 Multipliers

Four types of multipliers are possible using MOS transistors. Two of them use a two-transistor multiplying cell, and two of them a four-transistor cell. Several general conclusions applicable to all of the designs emerged from a computer analysis performed early in the program.

First, with large transistor geometries, perfectly matched threshold voltages and transconductances, and with proper and exact input voltages and biases, all four designs perform essentially perfectly. Second, when the channel lengths are reduced to 0.8 mil, small-channel effects result in a small non-linearity (less than 0.5 percent). The two-transistor differential multiplier has twice the output signal but the same percentage nonlinearity. The four-transistor dual-differential multiplier has a four times larger output signal, but again the percentage nonlinearity is the same.

The third general conclusion, applicable to all of the multipliers, is that a considerable voltage offset is required between the input signals applied to the drains of the multiplier transistors and those applied to the gates of the transistors.

The voltages on the gates must be large enough to ensure that the transistors are always in the linear region of operation. Table 5 lists input signal conditions that are adequate. A worst case (maximum voltage on drain/ minimum voltage on gate) offset of 2V is provided. As discussed in the section on source follower design that follows, separate bias rails have been used to permit the source follower offsets to be adjusted externally for satisfactory operation.

TABLE 5. INPUT SIGNALS USED IN EVALUATIONS OF MULTIPLIER CELLS

	Signals Applied To Gate Inputs	Signals Applied To Drain Inputs
Zero Reference	12 v	8 v
Peak Amplitude	1 v	1 v
Signal Range	11-13 v	7 to 9 v

Two-Transistor Reference-Balanced Multiplier

Computer analysis clearly showed two major weaknesses of this multiplier cell. The first is a severe dependence on the current summing bus bias levels compared to the zero-reference input signal level applied to the drain inputs. When the summing bus bias was reduced by a slight 0.1 V from 8.0 V to 7.9 V, the peak multiplier error increased from less than 0.5 percent to more than 10 percent.

The problem arises from the fact that the output of this circuit is the product of the gate input signal relative to its zero-reference value and the drain input signal relative not to its zero-reference but to the summing bus bias. If there were only one multiplier in the device, the bias on the summing bus could be adjusted. However, processing variations across a device can be expected to cause small differences in source follower characteristics (and hence zero-reference drain signal levels) from one end of the device to the other. It would then be impossible to get acceptable performance from all of the multipliers simultaneously.

The second major problem encountered was the output voltage distortion at the source follower outputs due to variations in the drain currents furnished to the multiplier. This effect will be referred to as "pulling" in the discussions which follow. For example, when the two-transistor multiplier cell was driven with the source follower described in Table 7 and using the input signal condition listed in Table 6 the maximum multiplier error was 0.2 percent when the multiplier transistors had an impractical W/L ratio of 0.001. For a more practical value of W/L of 0.25 (W=0.2 mil, L=0.8 mil), source follower pulling caused the peak error to soar to 13 percent.

TABLE 6. INPUT SIGNALS TO SOURCE FOLLOWERS USED IN ANALYSIS OF COMPLETE MULTIPLIER CIRCUITS

	Signals Applied to Followers Driving Gates	Signals Applied to Followers Driving Drain
zero reference	14 V	9.5 V
peak amplitude	1 V	1 V
signal range	13-15 V	8.5-10.5 V
approximate follower output zero reference level	11.5 V	7.5 V
approximate peak amplitude of follower output	0.9 V	0.6 V

Two kinds of pulling are involved. For a fixed input level to the source follower, changes in gate input signal cause the current drawn by the multiplier to vary. For a multiplier cell with W/L=0.25, the current drawn ranges overall from 25 μA of current sink to 21μA of current source. For a fixed drain input signal, the current variation with gate input signal is as much as 5μA. At a 12 kΩ output impedance, the source follower swings about 0.06 V or 10 percent of full scale.

The second kind of pulling results from the current changes as the drain signal varies, even with the gate signal held constant. To first order, this simply reduces the gain of the source follower. However, it also introduces a nonlinearity in the source follower. Analysis of the computer data showed a 4.2 percent maximum deviation when the gate input signal was held at its zero-reference value.

Because of these pulling effects, this multiplier could be used only if the current drawn could be substantially reduced and/or the source follower output impedance substantially reduced. Both changes would require transistors of much greater size (length in the case of the multiplier MOSFET's and width in the case of source follower driver FET's). This would be hard to achieve within the constraints of CCD pitch and chip size.

Two-Transistor Differential-Gate Multiplier

This cell was not examined in detail. It does nothing to alleviate the severe sensitivity of the reference-balanced cell to variations in offset between drain input level and summing bus bias. It does solve the problem of cross-pulling of the source follower by changes in the gate input signal. As the gate signal changes, the increase in current in one of the transistors is quite precisely balanced by a decrease in current in the other transistor with the inverted gate signal. In this respect, this multiplier cell is just one half of the dual-differential cell, and a complete discussion of the current balancing can be found under that heading. The self-pulling nonlinearity problem with the source follower is still present. For the added complexity of one differential-channel CCD, the circuit offers little improvement. The benefits of going to dual differential-channel CCD's are much greater.

Four-Transistor Reference-Balanced Multiplier

This cell also was not examined in detail. It overcomes the sensitivity to summing bus bias errors, but it suffers just as much as the two-transistor reference-balanced multiplier from self-pulling and cross pulling in the drain signal source follower. The simplicity of normal, nondifferential CCD channels makes additional real estate available for the larger transistors needed to solve the pulling problem (the area savings was

not enough to justify the inclusion of this approach in the correlator/convolver test pattern design, however).

Four-Transistor Dual-Differential Multipliers

This multiplier cell performed exceptionally well in the computer simulations, overcoming all of the problems uncovered in the other designs.

1) Summing bus bias: When the bias levels on the summing buses are shifted relative to the zero-reference level of the drain inputs, the main effect is to add a common-mode current to the two current buses. A secondary effect is a small change in the overall gain of the multiplier. For the input signal conditions described in Table 6 and with the current bus bias reduced to 7.5 (an offset of 0.5 V, five times greater than that applied to the two-transistor multiplier), the maximum deviations increased from 0.46 percent to 0.9 percent. Most of this was due to a gain increase of about 0.8 percent. Based on a new gain value, the maximum error of the multiplier was only 0.24 percent. Thus, the accuracy of the multiplier is actually improved when it is operated with the summing buses offset to a slightly lower voltage. This has the drawback of introducing common-mode current which would require better common-mode rejection in the differential current amplifier and might degrade signal-to-noise performance.
2) Source follower pulling: Under the signal conditions of Table 6 and with the drain-driving source follower load current at about 40μA maximum pulling of the source-follower output by gate-input changes was 0.00008 V (about 0.02 percent of full scale). The changes in the currents in the

paths with the normal and the inverted gate signals balanced each other to within 0.007μA. Perturbations in device geometries will result in less perfect cancelling in a real device, but errors larger by close to two orders of magnitude would still be acceptable.

The self-pulling of the source follower still results in a significant nonlinearity (4.6 percent) in its output. Nevertheless, the maximum error in the multiplier is only 0.15 percent. This is a dramatic indication of the extent to which the structural symmetry of the entire circuit nullifies nonlinearities in the individual circuit elements.

This is made even more dramatic when the load current in the source follower for the drain signal is cut in half to about 20μA. Under these conditions, the multiplier current load is between 19μA of sink and 17μA of source. The current through the driver transistor varies from 3μA to 40μA! The nonlinearity in the source-follower output is nearly 10 percent, and yet the overall multiplier accuracy is better than 0.8 percent.

When an offset of -0.55 V is added to the summing bus biases, the current through the driver transistor varies from 13μA to 56μA; the source follower linearity improves to 5 percent; and the overall multiplier error is less than 0.3 percent. This circuit was further analyzed with the input voltage swings increased from 2 to 3 V peak-to-peak. The drain signal zero-reference was raised to 10 V, and the VDD bias of the drain-signal source follower was increased from 10 to 10.5 V. Source follower nonlinearity with 40μA load current was 7.4 percent; overall multiplier error was a maximum of 0.4 percent.

3.2.2.2 Source Followers

Source followers are needed to buffer the outputs from the floating gate taps on the CCDs to the inputs of the multiplier circuit in order to prevent reverse coupling and to provide adequate drive capability. This is particularly true of the outputs that drive the drain inputs to the multipliers, since a steady current is required. The configuration of a source follower is shown in Figure 11.

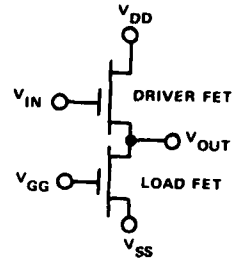


Figure 11. Schematic of Source Follower

The main design considerations are: linearity, drive capacity and power consumption. The source follower was analyzed first without any load. Nearly perfect linearity can be achieved provided the load and driver transistors are both maintained in the saturated region of operation. As a rough rule of thumb, this means that VGG is below the minimum value of Vout and VDD is above the maximum value of V_{IN}. Power is minimized when VGG and VSS are as close as possible, but a reasonable margin is required between VGG and VSS to prevent small variations in threshold voltage from seriously affecting the load current level.

As mentioned earlier, the analysis of the performance of the multiplier cells showed that a considerable offset is required between the voltage levels applied to the gates and those applied to the drains. Obtaining the lower voltages from the drain-driving source followers by using a small W/L ratio for the driver and pulling a large current through it was considered. This, however, results in high power consumption and cannot give an adequate offset. It was decided instead to offset the clock voltages at which the floating gates of the two CCDs are driven. This does not affect CCD performance, achieves a larger offset, and is adjustable externally (without mask changes).

The source follower parameters listed in Table 7 were chosen for the subsequent analysis. They are consistent with the requirements of the layout and design rules, and adjustments in the bias and supply voltages permit satisfactory operation over a wide range of conditions.

TABLE 7. SOURCE FOLLOWER PARAMETERS CHOSEN AS A RESULT OF COMPUTER ANALYSIS

Parameters	Source Followers Driving Gates	Source Followers Driving Drains
driver FET width	0.5 mil	0.5 mil
driver FET length	0.2 mil	0.2 mil
load FET width	0.4 mil	0.4 mil
load FET length	0.8 mil	0.4 mil
VDD	14 V	10 V
VBB	11.5 V	7.5 V
VSS	8.4 V	4.8 V
approximate load current	20μA	40μA
power dissipation (no external load)	110μW	210μW
output impedance (no external load)	18kΩ	12kΩ
input signal range	12.5 - 15.5	8 - 11 V

3.2.3 Parameter Variation Sensitivity Analysis

The sensitivity of the correlator/convolver performance to parameter variations was also investigated using computer models. The most critical parameters are expected to be the 0.2 mil channel widths in the multiplier transistors and the 0.2 mil channel lengths in the source follower drivers. The effects of variations in these values were studied by calculating the effect of exaggerated errors.

Drain-Driving Source Follower

When the channel length of the driver transistor in one of the two source followers whose outputs feed drains of the multiplier transistors was increased by 1μm (20 percent), the overall multiplication accuracy was degraded to 6.4 percent, an error that appears almost entirely as a feedthrough of the signal applied to the multiplier gates. The change in transconductance in the source follower has two effects. One is a change in gain of about 6 percent and the other is a change in the zero-reference output

level of about 75 mV or 12 percent of the signal amplitude. Analysis of the 4 transistor multiplier alone shows that the gain error contributes no measurable degradation in accuracy; the error arises entirely from the offset error, half of which appears as common mode and is rejected and half of which appears as normal mode where it acts as a dc drain signal. In the 2 transistor multiplier, which lacks common-mode rejection, the error under the same conditions is nearly twice as large.

One can expect a reduction in error if the minimum geometries are increased. For example, the channel length in the driver transistor can be increased to 0.4 mil provided some dc bias conditions are adjusted. A 1μm increase in channel length is now only a 10 percent error. The multiplier error decreases by about one quarter to 4.7 percent. The reduction is less than one half because the impedance level increases. One pays a power penalty because the V_{DD} to V_{SS} voltage drop is larger, and, if the transistor geometry becomes too large, one encounters problems in routing conductors around the transistors. However, should we encounter difficulties with our present dimensions, some room for reducing error sensitivity is available.

Gate-Driving Source Followers

If the same variation is applied to the transistors in the source followers driving the gates of the multiplier transistors, the effect and its cause are the same except that the error now consists of feedthrough of the drain signal.

Multiplier Transistors

When the 0.2 mil width of one the multiplier transistors is increased by 1μm (20 percent), a much larger error appears in the simulation, about 17 percent. This error consists of feedthrough of the drain signal. When this feedthrough signal is removed, the residual error is less than 1 percent.

The current in the modified transistor is, to first order,

$$I = (g_m + \Delta g_m) \left[(V_G^{SIG} + V_G^{(0)} - V_{TH}) V_D - 1/2 V_D^2 \right]$$

The change in current due to the change in g_m is:

$$\Delta I = \Delta g_m V_G^{SIG} V_D + \Delta g_m (V_G^{(0)} - V_{TH}) V_D - 1/2 \Delta g_m V_D^2$$

The usual total output current from the 4 transistors together is $4 g_m V_G^{SIG} V_D^{SIG}$. The first term represents a modest fractional gain change of $1/4 \frac{\Delta g_m}{g_m}$. The second term is the source of the large feedthrough of the drain signal. It represents a peak error to peak signal ratio of:

$$1/4 \frac{\Delta g_m}{g_m} \quad \frac{V_G^{(0)} - V_{TH}}{AMP}$$

Where AMP is the amplitude of the input signals. Since $V_G^{(0)}$ must be offset from V_{TH} by at least twice and typically three to four times AMP, this term becomes very large. Clearly, its effect is minimized by operating with as little gate signal offset as possible.

The final term is the small residual quadratic distortion. The results of the computer simulation show less of this distortion than the above equation predicts.

Conclusions

Geometrical variations in the source follower transistors introduce inaccuracies into the multiplier output as a result of offsets in the zero-reference level outputs. To achieve 1 percent accuracy, these offsets must be held to the order of 10 mV. Transconductances among the source follower transistors associated with each differential CCD must be held within about 3 percent, a figure that probably can be achieved. If not, the minimum device dimensions can be increased somewhat. It should also

be mentioned that feedthrough errors are among the least critical for most applications because the error signals will add incoherently along the 256 stages of the correlator, and an effective processing reduction on the order of $256^{-1/2} = 1/16$ can be expected.

The sensitivity of the selected multiplier to offset errors in the signals applied to its inputs points up another problem which is in all likelihood more serious than that of balancing the two source followers. This is the inevitable dc imbalances between the two halves of each differential CCD. Large clock feedthrough signals occur because of capacitive coupling between pairs of lines. It is therefore, imperative that independent biasing controls be maintained over the two halves of the CCD' s. In the correlator on the test chip we will bring out most clock and bias lines independently.

The selected multiplier is especially sensitive to variations in transconductance because of the $V_G^{(0)} - V_{TH}$ amplification factor. However, the 4 transistors in the multiplier cell are in very close proximity and oriented in such a way that parametric variations between them will be minimized (see Subsection 3. 3.).

All of the effects described above are no greater in the 4-transistor multiplier than they would be in a 2-transistor multiplier with minimum-geometrical features that are twice as large. Thus there is no sacrifice in performance in going to the 4-transistor cell, the fine geometrical features notwithstanding.

3.3 Mask Design

3.3.1 General

Figures 12 through 14 show the mask layouts of the principal parts of the CCD correlator/convolver. The overall plan of the correlator places the multipliers in the center and the two tapped differential CCDs on each side of the row of multipliers. One of the differential CCDs drives the multiplier drain inputs and the other drives the multiplier gate inputs.

The CCD correlator/convolver was designed using depletion devices exclusively for simplicity. Major attention in both circuit design and mask design was given to minimizing the effects of parameter (threshold voltage and g_m) variations upon the accuracy of the correlator/convolver.

All transistors have gates formed from the first level of polysilicon so that process and operating temperature variations will not affect device tracking. Although the circuit configurations and mask design approach used can help greatly to reduce errors due to such systematic effects, random variations are more difficult to compensate for in this manner. Process experiments to reduce random variations of threshold voltage and transconductance across the wafer will be performed in 1979 if more uniform characteristics are shown to be essential to achieve acceptable correlator/convolver characteristics. In addition, mask design changes could be made to alter device geometries, if necessary.

3.3.2 Multiplier

Figure 12 shows the multiplier mask design for the correlator/convolver. The four transistors in a given multiplier have been arranged with the same orientation and along a straight line. Mask alignment errors in either direction will, therefore, affect all transistors identically and will have no affect on multiplier accuracy. Furthermore, the circuit connections to the four transistors have been made in a way that compensates for constant gradients in transconductance and threshold voltage. Figure 15 shows schematically the circuit layout with the four transistors spaced at equal distances, d. The analysis for transconductance variations proceeds as follows.

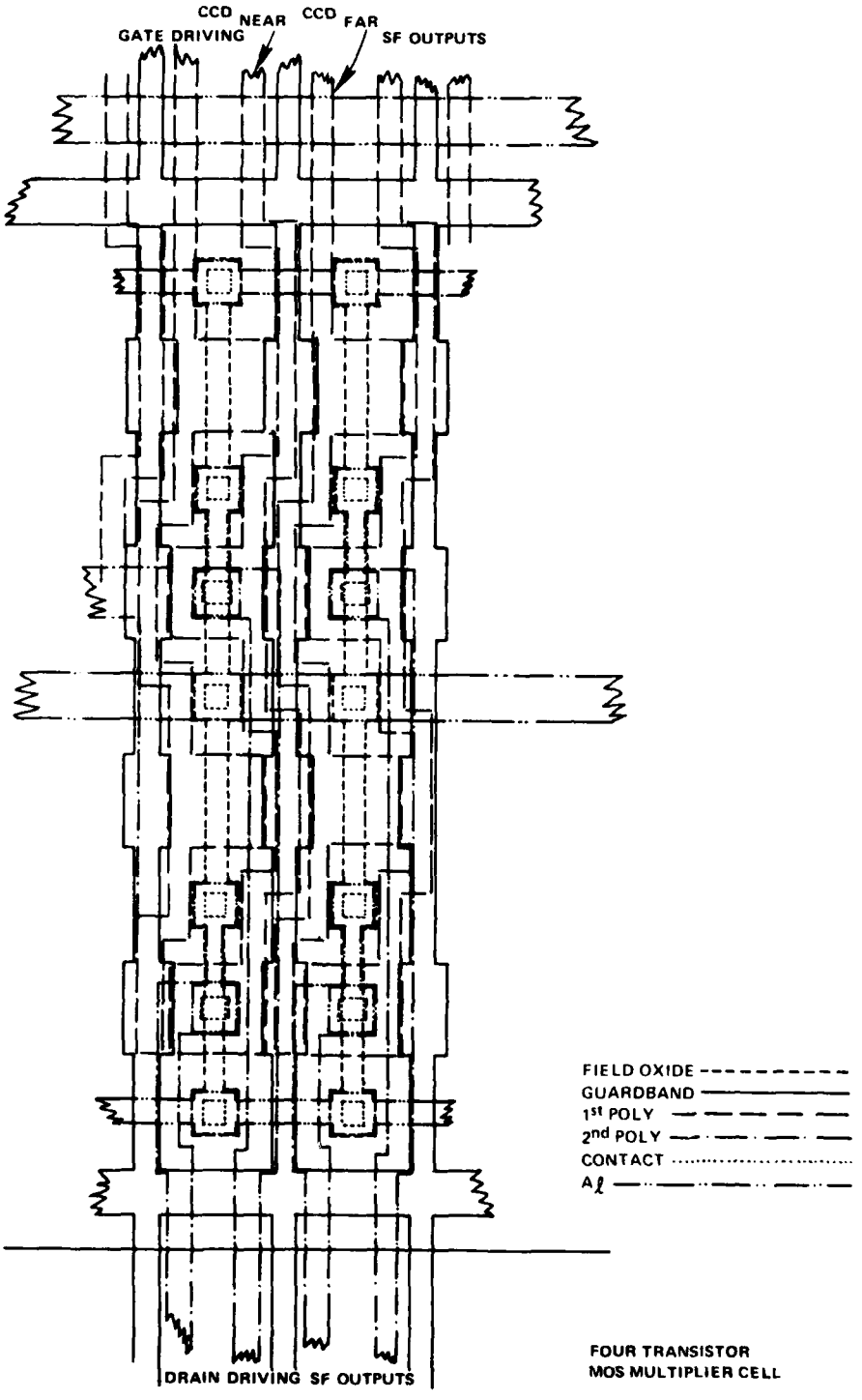
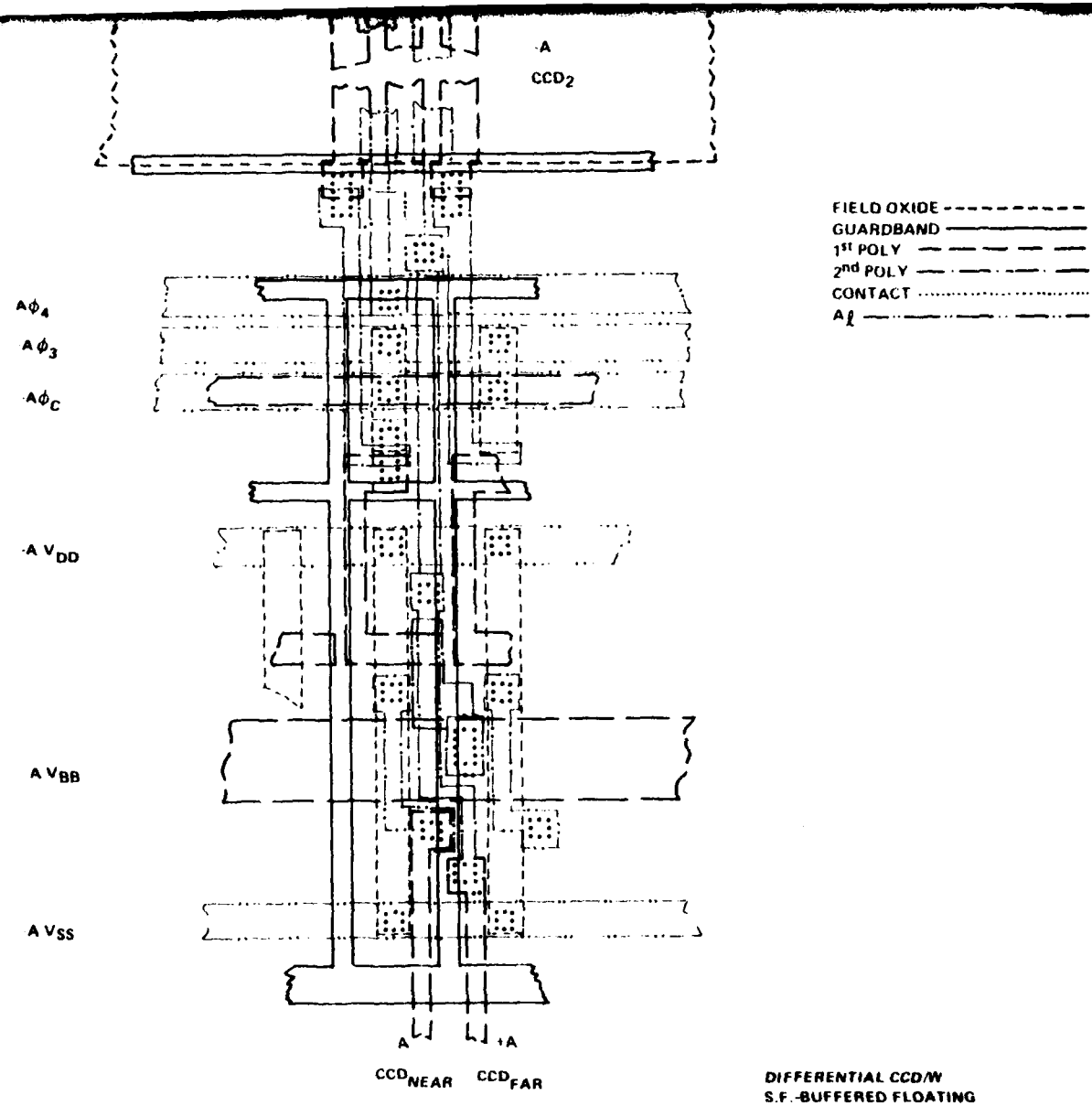


Figure 12. Four-Transistor MOS Multiplier Cell



DIFFERENTIAL CCD/W
S.F.-BUFFERED FLOATING
GATE TAPS

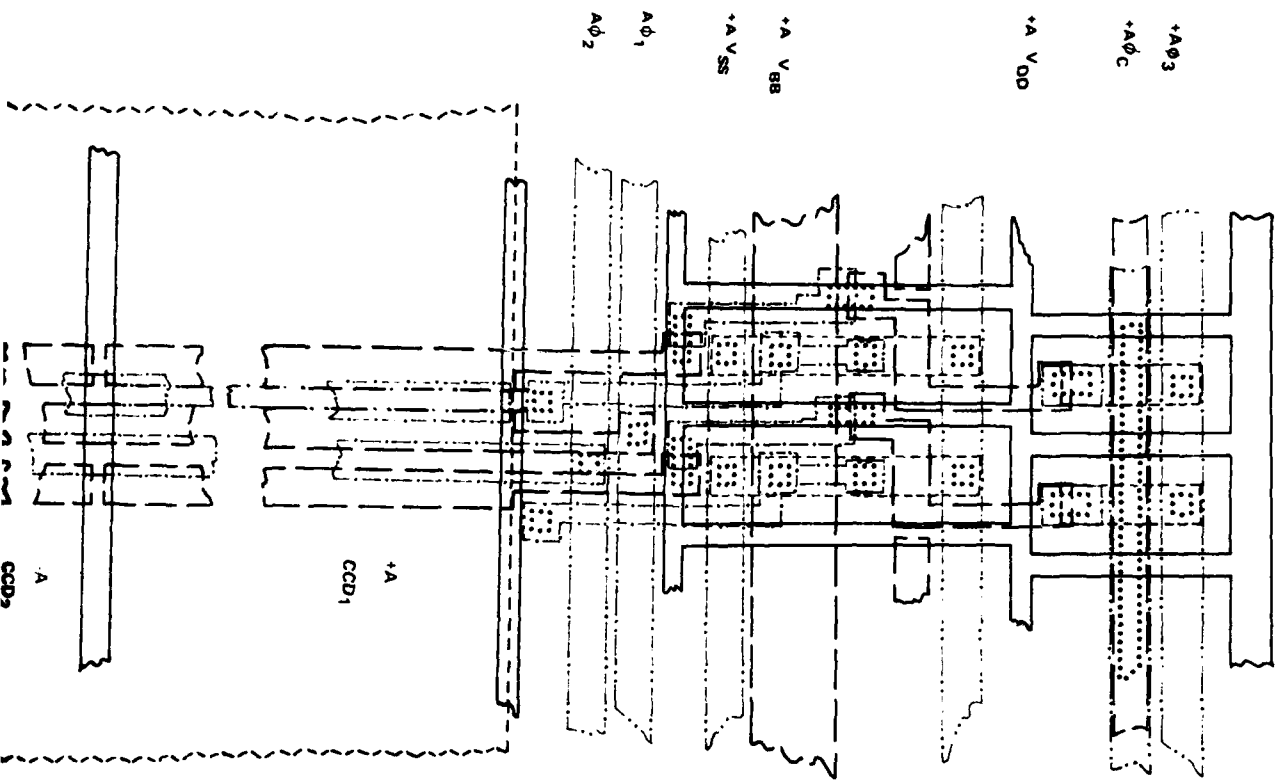


Figure 13. Differential CCD/W SF Buffered Floating Gate Taps

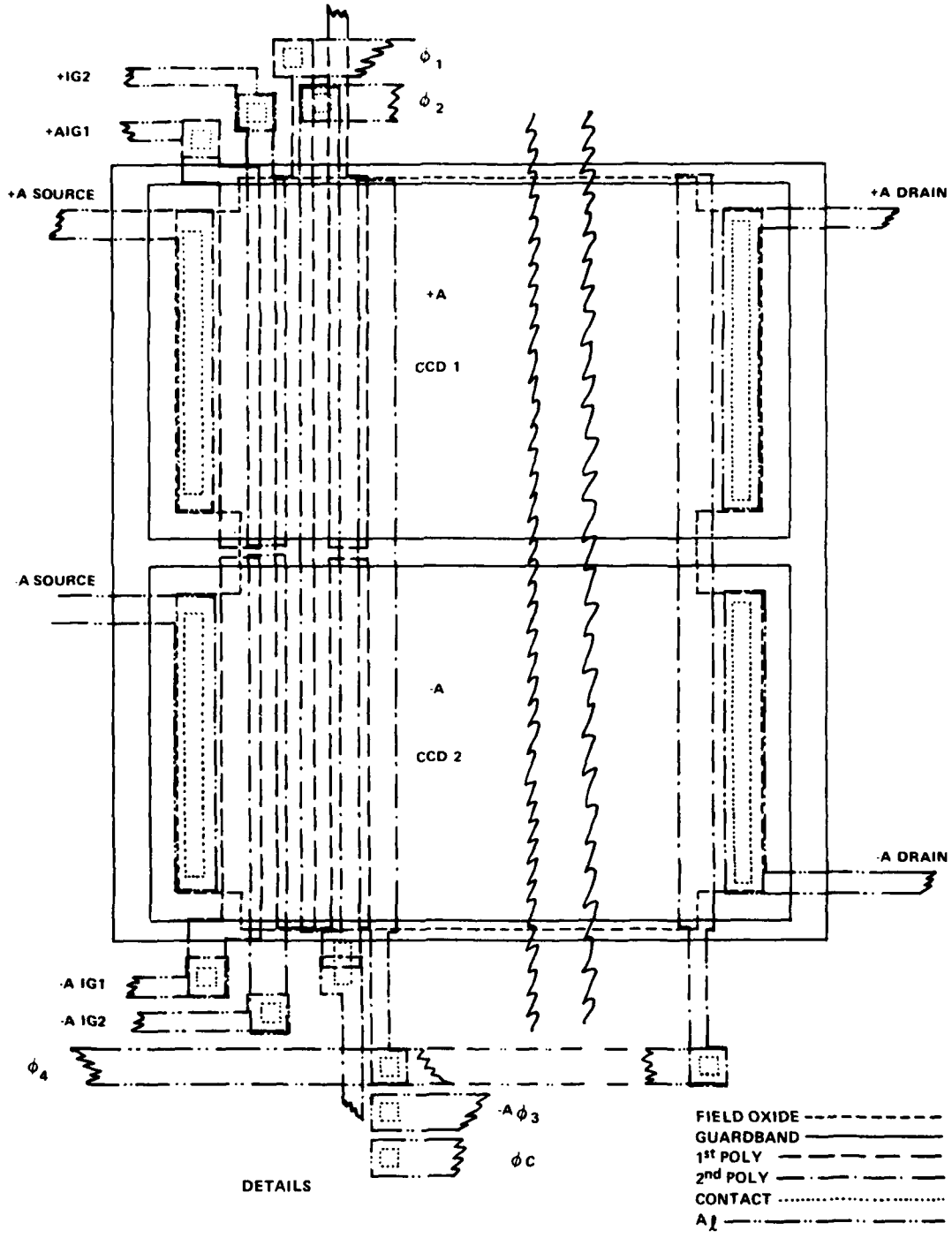


Figure 14. Differential CCD Source/Drain Details

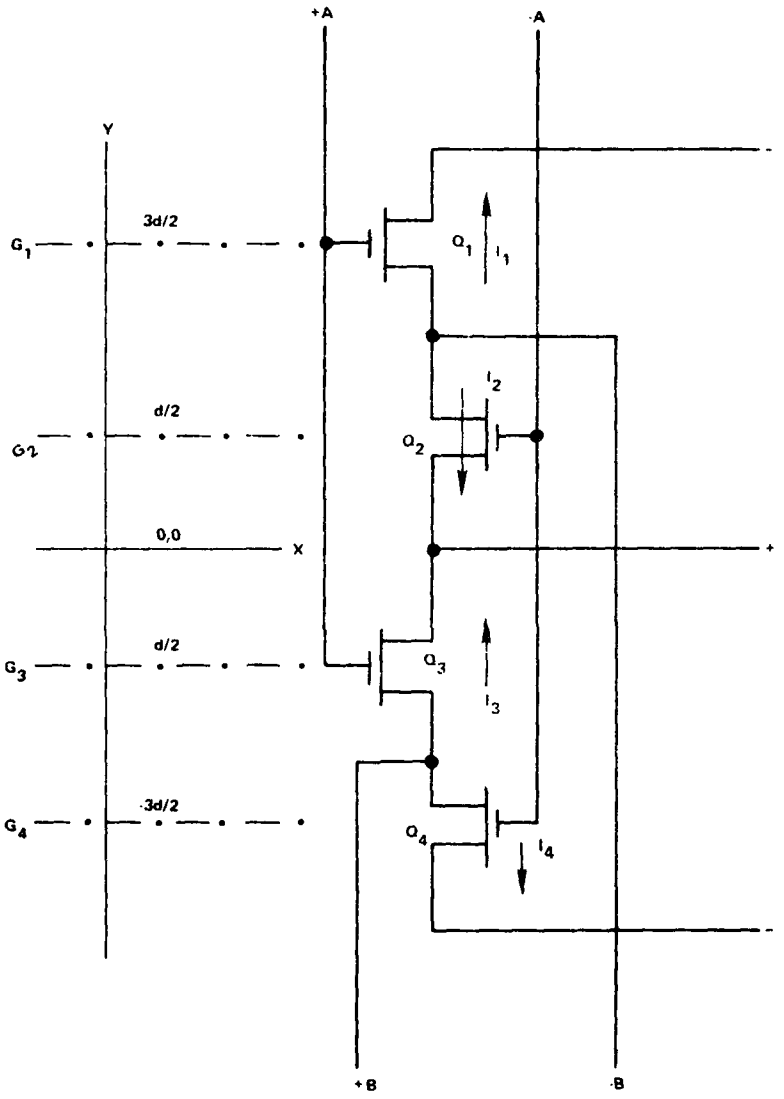


Figure 15. Four-Transistor Multiplier Schematic

If the center of the string is selected as the origin and the transistors are assumed to vary their transconductance linearly with distance, the currents in the devices are approximately (assuming identical threshold voltages):

$$I_1 = KA(-B)(1 + 3/2d\Delta)$$

$$I_2 = K(-A)(-B)(1 + d\Delta/2)$$

$$I_3 = KAB(1 - d\Delta/2)$$

$$I_4 = K(-A)B(1 - 3d\Delta/2)$$

where

- K - device transconductance
- A, B - input voltages
- d - distance between gates
- Δ - relative change of K with position

When these currents are summed to form the output $I_{OUT} = -I_1 + I_2 + I_3 - I_4$, all Δ terms cancel and the net current is $I \approx KAB$ (4).

3.3.3 Tapped Differential CCD

Figure 13 shows the mask layout of the differential CCD portion of the correlator/convolver as provided for the gate driving inputs to the multiplier. The drain driving differential CCDs are located on the opposite side of the row of multipliers and, except for the increased transconductance of the source follower load devices, is the mirror image of Figure 13. The source follower outputs from the outer floating gate taps must be passed undisturbed over both CCDs to the multipliers on the centerline of the chip. This is done by using aluminum interconnect over the Phase 4 clock phase, which, when four-phased clocking is used, remains static during the charge transfer to the floating gates and the readout time which follows. With two-phase clocking, both clocks are static during the readout time.

The widths of the CCD channels are not shown to scale in Figure 13. They are relatively wide (15.5 mil) so that the capacitive loading of the interconnection to the source followers will be relatively small. Since the source follower outputs from the outer CCD channels must cross the input circuitry

of the inner source followers, it is impossible to have exactly symmetrical layouts for the outer and inner amplifiers. The parasitic capacitors involve six different oxides. The tracking of each contribution to the floating gate parasitic capacitance had to be considered carefully. To achieve uniformity between the taps on different CCDs, the design must rely partially on making the unmatched parasitic capacitance a small part of the total floating gate capacitance.

Unfortunately, the mask design of the differential CCDs could not provide compensation for nonrandom offset voltage variations between the four source follower outputs in the manner shown earlier for the four transistor multipliers. The use in the 32 stage prototype correlator of independent biasing for the four rows of source follower loads will permit the effects of such variations to be minimized by adjusting outside bias supply levels separately. (Note: This is not suggested as a permanent solution to the problem, which may not be all that serious.)

Figure 14 shows the mask design of the input and output ends of the existing differential CCDs. Two gate inputs are provided and the output is, for the sake of simplicity, just a diffusion. The test pattern was not fitted with the two sets of input gates which would be required for combined correlation/convolution operations since this would require additional pins and it was considered to be more important to have separate access to many internal bias and clock lines on the chip. No problem is anticipated in incorporating the extra gates in the final correlator/convolver mask series, however.

3.3.4 Test Mask Layout

Figure 16 shows the overall plan of the test mask layout. Note that it largely is made up of 68 mil square patterns. This was done to use the standard 28 pin probe card currently in use at the Raytheon Missile Systems and Research Divisions for CCD, MOSFET and MESFET process test patterns. The test mask has eight individual patterns in it, as itemized in Table 8. All eight patterns in the test mask are described in detail in the sections which follow along with the rationale for their design.

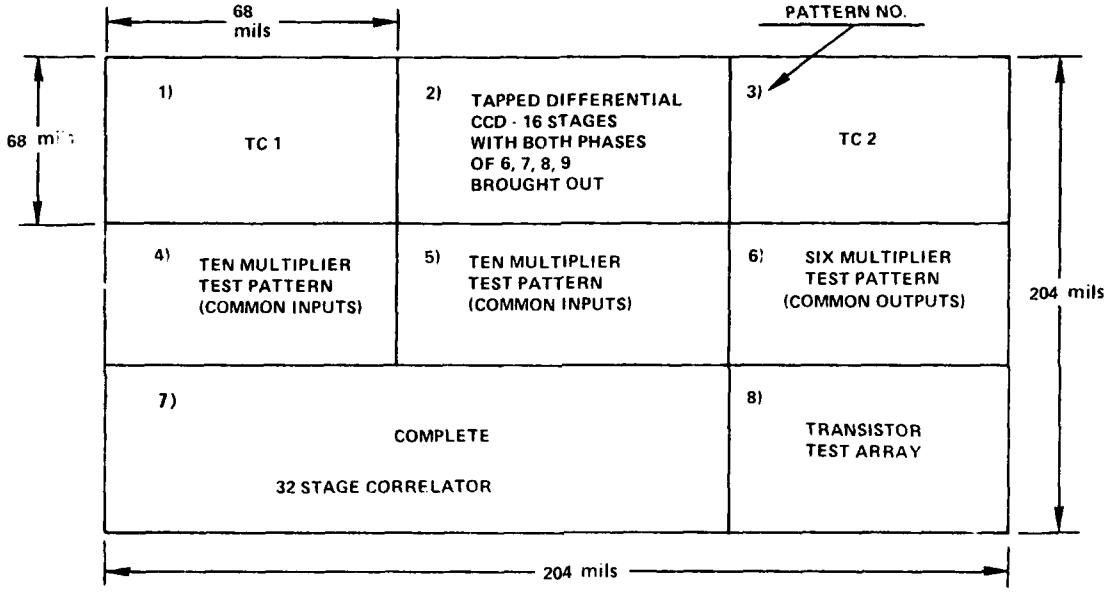


Figure 16. CCD Correlator/Convolver Test Mask Plan

TABLE 8. TEST MASK PATTERNS

Test Pattern No.	No. Pads	Description
1	34	TC1 Standard Raytheon Test Pattern for poly/poly surface/buried channel CCD. Includes patterns to evaluate capacitors, contact chains, GB to S/D breakdown, interconnection continuity over steps
2	34	Sixteen stage tapped differential CCD with + and - tap outputs for Stages 6, 7, 8 and 9 (Drain Driving Version)
3	50	TC2 Standard Raytheon Test Pattern for poly/poly surface/buried channel CCD. Includes patterns to evaluate capacitors, contact chains, gated diodes, resistors, interconnection continuity over steps and transistors with implant and geometry variations
4	34	Ten four-transistor MOS multipliers with inputs in common and separate outputs on 1.2 mil centers
5	34	Ten four-transistor MOS multipliers with inputs in common and separate outputs on 1.2 mil centers
6	28	Six four-transistor MOS multipliers with outputs in common and separate inputs on 1.2 mil centers
7	44	Thirty-two Stage Correlator with independent bias and clock lines for all functions (except first CCD gates are paired for Ref and Signal CCD)
8	56	Six Test Transistors each of seven types on 1.2 mil centers

The placement and composition of the cells used in the test mask patterns were arrived at, keeping in mind the potential sources of parameter variations in finished correlator/convolver chips. The chief parameter variations to be considered included threshold and transconductance variations in the MOS transistors and the storage well and parasitic capacitance variations associated with the floating gate taps. In addition, the IR drop of the polysilicon interconnects had to be considered. The reason for the composition and placement of the cells in each test pattern will be considered in turn in the paragraphs which follow.

Pattern No. 1

This test pattern is the TC 1 standard pattern used with the Raytheon poly/poly surface/buried channel CCD wafer fabrication process. It is described in sufficient detail in Table 8 and is located at one corner of the test mask plan shown in Figure 16. Since no attempt will be made to measure minute parameter variations between TC 1 and the correlator/convolver test patterns its location was noncritical. This pattern is 68 mils square and has 34 contact pads, 28 of which are located on the chip edges for automated process monitor testing.

Pattern No. 2

This test pattern consists of 16 stages of the differential CCD portion of a complete correlator/convolver. Since the distortion and accuracy errors associated with the differential CCDs which drive the MOS multiplier drains are expected to far exceed those of the gate driving differential CCDs, only the drain-driving CCD is in the test mask in this pattern. The pattern consists of 16 stages with the buffered outputs from both halves of the channel brought out at Stages 6, 7, 8, and 9. This pattern will enable the measurement of tap-to-tap variations of adjacent taps directly on the actual 1.2 mil pitch of the finished correlator/convolver. Longer distance variations can be measured by comparing adjacent test patterns, which will be on 204 mil centers. This test pattern also contains 0.2 mil wide first poly, second poly and aluminum runs, since these are used for interconnection in all of the cells

of the correlator/convolver and are not available on TC 1 and TC 2. This test pattern is 68 mils square and has 34 pads, 28 of which are on the pattern edges for automated characterization tests.

Pattern No. 3

This test pattern is the TC 2 standard pattern used with the Raytheon poly/poly surface/buried channel CCD wafer fabrication process and described in sufficient detail in Table 8. Its placement was also considered noncritical. It is 68 mils square and has 50 contact pads, 28 of which are located on the chip edges for automated process monitor testing.

Pattern No. 4

This test pattern consists of 10 four-transistor multipliers on 1.2 mil centers with common inputs and isolated output nodes. It will enable the accuracy of each multiplier to be evaluated separately. Unfortunately, some polysilicon interconnect geometry changes had to be made to achieve separate outputs, and this led to generation of test pattern No. 6.

This test pattern also includes an "ideal" four-transistor multiplier with very large (2 mil x 2 mil) dimensions. Also included are contact chains of first poly, second poly, and N+ with the 0.2 x 0.2 mil openings and 0.1 mil overlaps similar to those used in all the correlator/convolver cells. These have been included since the existing contact chains in the TC 1 and TC 2 test patterns were designed using more conservative mask layout rules.

Pattern No. 5

This test pattern is identical to Pattern No. 4 and is provided so that variations in device geometries due to the location in the optical field of the chip can be detected and evaluated.

Pattern No. 6

This test pattern consists of six multipliers with common outputs and separate inputs exactly as they would appear in a finished correlator/convolver to permit assessment of any variations in multiplier accuracy due to the rearrangement of interconnects in the other multiplier test patterns.

This test pattern is 68 mil square and has 28 pads on the edge of the chip for automated characterization testing.

Pattern No. 7

This test pattern consists of an entire 32 stage correlator with separate clock and power supply connections brought out for each portion of the device layout. It will allow an early assessment of problems that may occur due to interconnecting the correlator/convolver elements and permit a study of the interaction of power supply and clock waveform variations on correlator performance.

The pattern is 68 mil by 136 mil in size and has 44 pads located on its outside edges for characterization tests.

Pattern No. 8

This pattern is a test transistor array consisting of seven different transistor types located in rows of six on 1.2 mil centers. The devices in the array consist of the following types:

1) Four geometries of multiplier transistors so that the variations in multiplier transistor characteristics can be compared as a function of geometry. The following transistor geometries are included:

Width (mil)	Length (mil)	
0.2	0.8	(as used in multiplier currently)
0.2	1.6	
0.4	0.8	
0.4	1.6	

2) In addition, this test pattern includes clusters of six transistors on 1.2 mil centers identical to those used for the source follower drivers, drain-driving source follower loads, and gate-driving loads in the floating gate output circuits of the differential CCDs.

This test pattern is 68 mil square and has 56 pads for automated characterization testing.

3.4 Process Design

3.4.1 General

The wafer fabrication of the correlator/convolver was originally expected to be performed using the existing standard Raytheon CCD process. When the cells for the correlator/convolver were designed, however, it was discovered that a considerable performance penalty would result (as well as large chip area) if the device were to be built using the existing layout rules (7.5 μm poly and alumunium line widths and spaces) compared to what could be achieved using a more advanced process.

As a result, the layout rules were revised to permit 5μm poly and aluminum lines with 2.5 μm spacings. The revised rules were then incorporated into the design of the correlator/convolver test pattern.

Although resolution pattern data indicated that the new denser layout rules could be achieved with a conventional guardbanded thick oxide process using the new projection aligner, it was expected that superior results would be achieved using a coplanar process. The coplanar process would provide lower steps for the polysilicon and aluminum to cover and also improve the ability of photolithography to define them.

It was therefore decided to make some experimental correlator/convolver test patterns using the coplanar isolation technique as well as some using the conventional thick oxide guardbanded process.

The new coplanar process, which will be described in detail later, would use a relatively low concentration p-type implant which would come up right to the edge of the device areas and be adjacent to source, drain and channel areas. The existing thick oxide etch mask would be used to define nitride covered device islands, surrounded by etched back silicon, and then a boron implant would be used to create a lightly doped guardband area everywhere but in the device regions. This would be followed by growth of the coplanar field oxide such that the field oxide would have a lightly doped p layer under it for guard band purposes.

The following subsections will describe the characteristics of the original Raytheon CCD process and how it was modified for use in this program for both conventional guardbanded and coplanar wafer fabrication.

3.4.2 Process Development

The fabrication of the correlator/convolver test structures was based mainly on our standard CCD process which had yielded excellent results in the past in terms of device performance and die yield. In conjunction with an implanted buried channel, this process has enabled us to make 64 stage 60 MHz, two phase CCD structures with die yields of 40-50 percent. The special features of the process are:

1) Three levels of conductors - The first and second consist of 5000 Å thick phosphorus-doped, oxidized polysilicon and the third one consisting of a composite of 2000 Å of phosphorus doped polysilicon with approximately 5000 Å of aluminum on top. This composite third conductor is formed by using a single photoresist masking step.

   The polysilicon portion of the third conductor layer protects shallow doped regions such as sources and drains against alloy formation with the aluminum, and since it is chemically vapor deposited, it greatly improves step coverage.

2) Self-registered polysilicon gates with source and drain regions formed by implanting phosphorus through gate oxide - This technique is superior to implanting into source and drain regions with the gate oxide removed from them, because no oxide undercutting under the gate occurs and less damage is produced by the ion implant.

3) Phosphorus diffused polysilicon - This has a lower sheet resistance (typically 25 Ω/square for a 5000 Å thick layer) than can be achieved with implanted phosphorus, even at high implant doses ($\geq 2 \times 10^{15}/cm^2$).

4) Shallow source and drain contact regions - These reduce space requirements and parasitic capacitances and are made possible by the use of the composite third conductor layer.

5) Optional diffused guardband or coplanar oxide isolation - Either can be easily implemented in the processing without the need for additional masks.

6) Gettering by implanting BF_2 into the back of the wafer, This implant also ensures a good electrical contact to the wafer.

High temperature processing was done in polysilicon furnace tubes periodically cleaned with HCl gas. The field oxide used in the coplanar process was formed in an environment produced by reacting hydrogen with oxygen. All other oxides were formed in an ultradry atmosphere derived from a liquid oxygen supply. Supply lines were carefully leak checked, and the gases were passed through submicron filters. Hydrogen chloride was added to the atmosphere for wet oxidation and trichlorethane (C33) to the atmosphere for dry oxidation to ensure the highest possible cleanliness of the oxides. Extensive use was made of a plasma etcher (barrel-type with aluminum cage) to etch the polysilicon and the silicon nitride layers and to remove photoresist after etching and residues after development.

Conventional contact printing was used for the photolithography with a registration accuracy close to 1.5 μm. The chemical processing was performed with electronic grade chemicals, and with 18MΩ water prepared by reverse osmosis and passed through a 0.2 μm filter. The resistivity of the effluent rinsing water was monitored and allowed to reach 16MΩ before the wafers were taken from the rinsing bath. For this work, we used boron doped silicon wafers from two different vendors: Dow Corning (8-51 Ω-cm) and Monsanto (10-40 Ω-cm).

3.4.3 Mask Steps

The following masking steps were used:

- Mask No. 1 - Guard Bands (not used in coplanar process)
- Mask No. 2 - Field Oxide (defines guard band in coplanar process)
- Mask No. 3 - MOSFET Gates and CCD Phases 1 and 3
- Mask No. 4 - Interconnects and CCD Phases 2 and 4
- Mask No. 5 - Via Holes
- Mask No. 6 - Final Interconnects

SECTION IV
RESULTS

4.1 General

The results which follow are based upon a number of wafer fabrication runs in three wafer fabrication phases.

The first phase was performed early in the program to evaluate the coplanar oxide isolation technique and to verify the design rules chosen for its implementation.

The second phase used the initial version of the correlator/convolver test pattern mask series. This cycle produced working multipliers, but mask and processing problems precluded quantitative evaluations of the remaining patterns.

The third processing phase incorporated corrected masks and process improvements. Working versions of all patterns have been seen including CCDs and full correlators. Specific data will be presented in the sections that follow.

Figures 17 through 19 are photomicrographs of the overall pattern, the 32 stage correlator, and the bridge multiplier section of the 32 stage correlator taken from completed wafers.

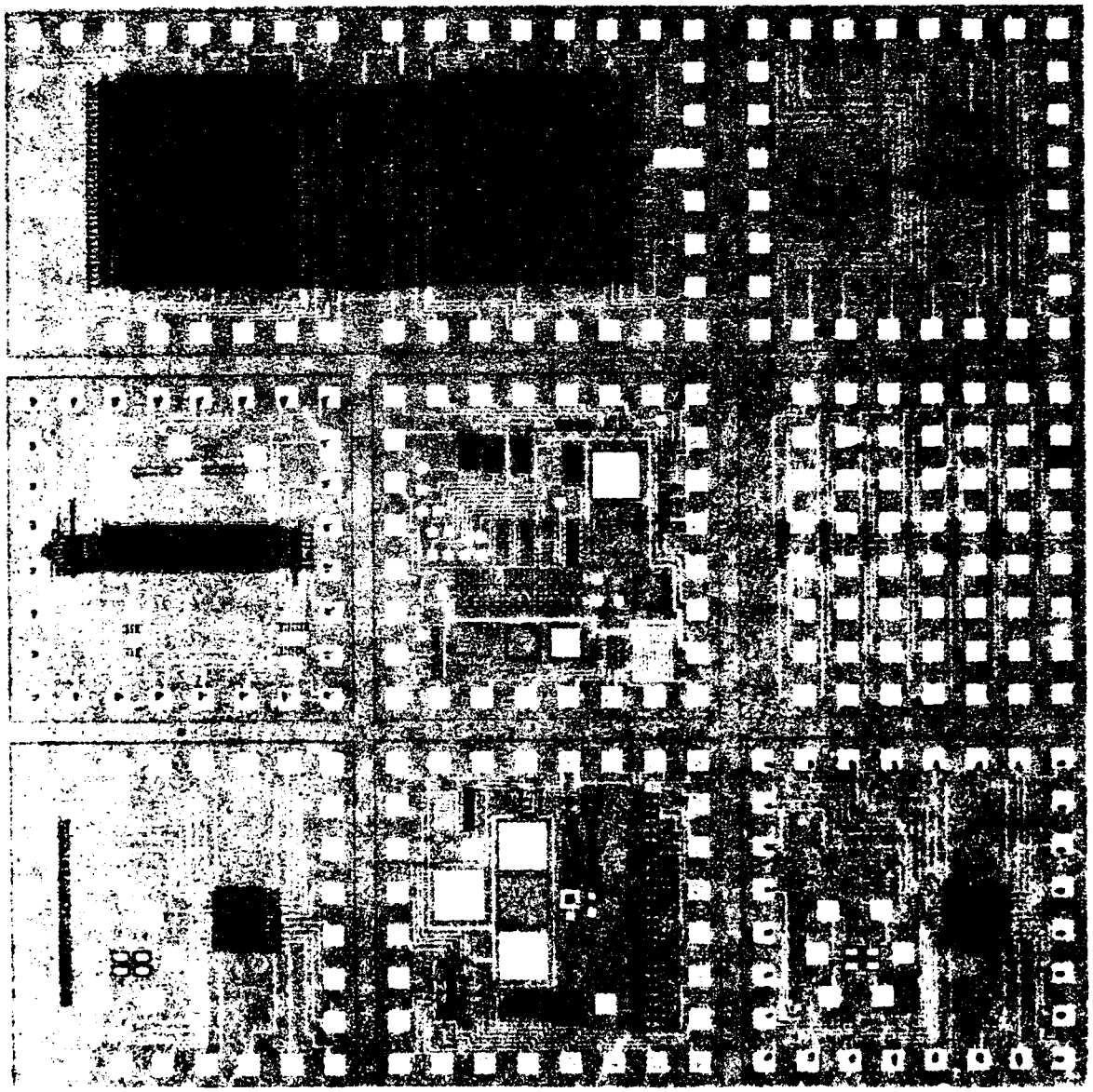
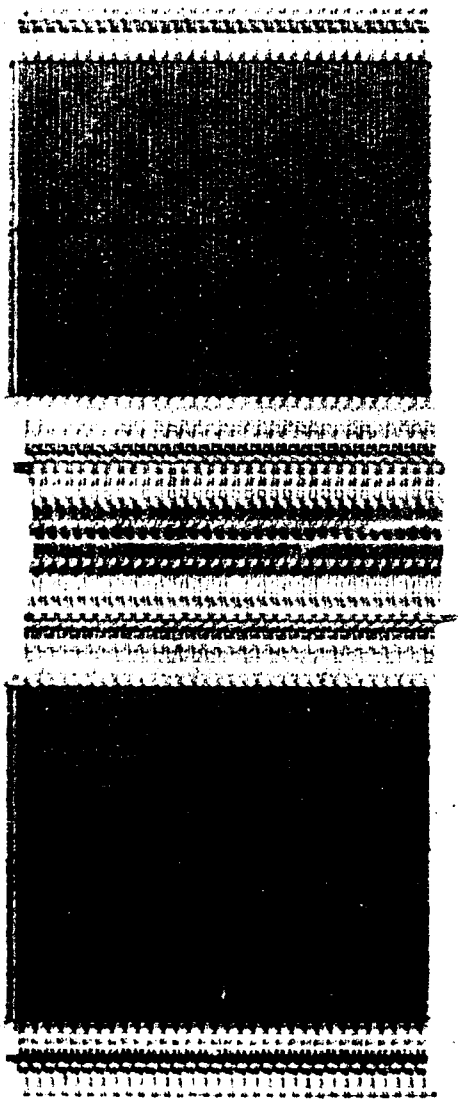
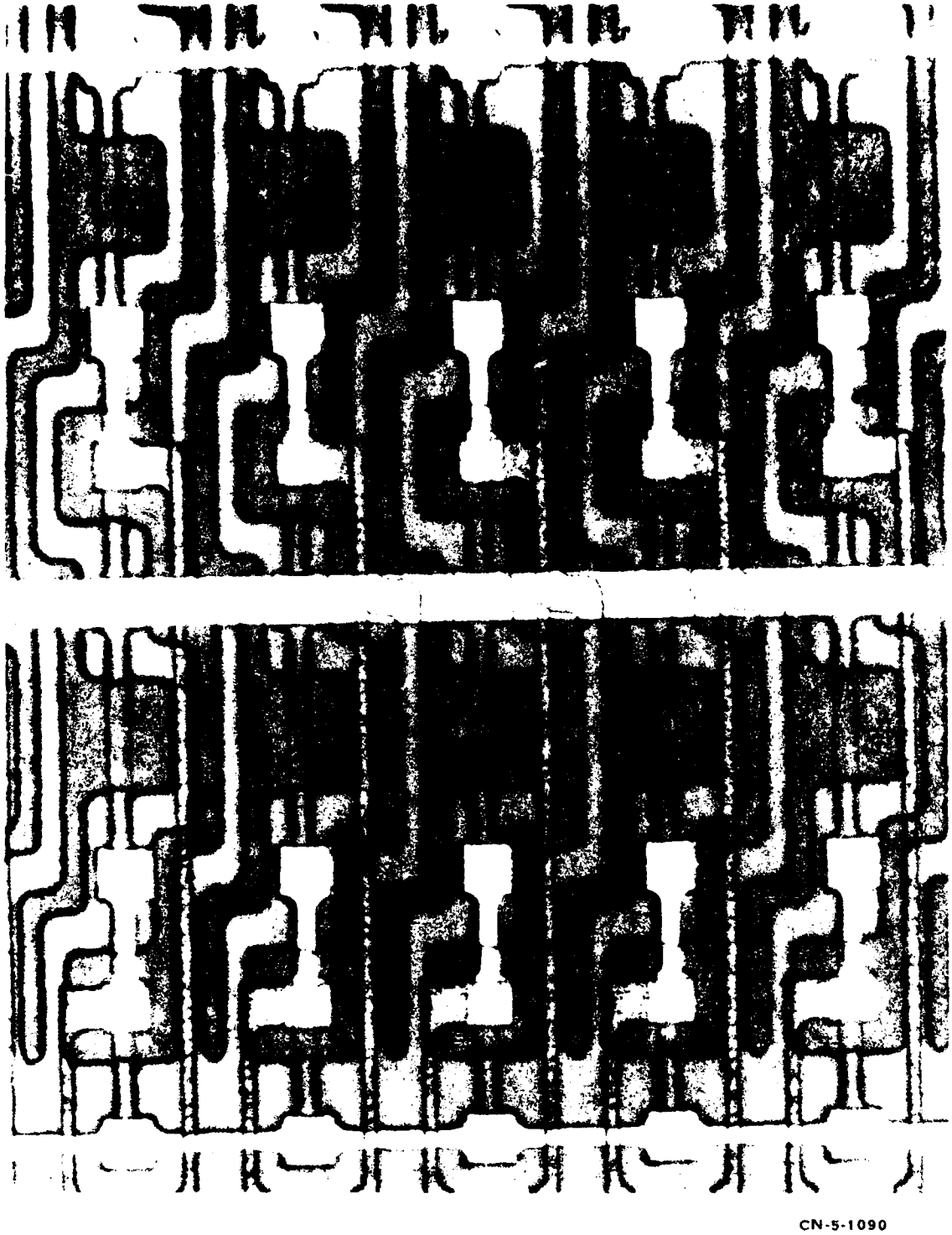


Figure 17. Correlator/Convolver Test Pattern Photomicrograph (Approximately 34X)



CN-5-1089

Figure 18. Thirty-Two Stage Correlator Photomicrograph (Approximately 46X)



CN-5-1090

Figure 19. Bridge Multiplier Photomicrograph (Approximately 1200X)

4.2 Coplanar Isolation

Since the coplanar structure was expected to make fabrication of the 5 x 5 μm contacts and polysilicon and aluminum interconnects on 7.5 μm centers much easier, preliminary investigations of the new wafer fabrication steps needed were carried out early in the program. The coplanar process uses a silicon nitride oxidation barrier over the areas which will become active devices. The isolation areas are etched down by about one half the final field oxide thickness. Boron is lightly implanted into the isolation regions before the oxide is grown. Because of the lighter boron concentration, it is permissible to have the guardband form a junction around the transistor sources and drains without encountering an unacceptable reduction in isolation breakdown voltage. With conventional highly-doped diffused guardbands, a buffer of high-resistivity material must surround the source and drain regions.

Experiments with the coplanar process were conducted using both isotropic and anisotropic etching, etching depths from 0.3 to 0.45 μm, and boron doses from 3×10^{13} to 1.5×10^{15} per cm^2. In all cases the final field oxide thickness was approximately twice the initial etch depth. The results of this work were used to create the curve shown in Figure 20 of isolation breakdown voltage versus boron dose. In view of these results, we adopted a 0.5 μm etch depth and 10^{14} cm^{-2} implant dose for the coplanar oxide isolation version of the correlator/convolver.

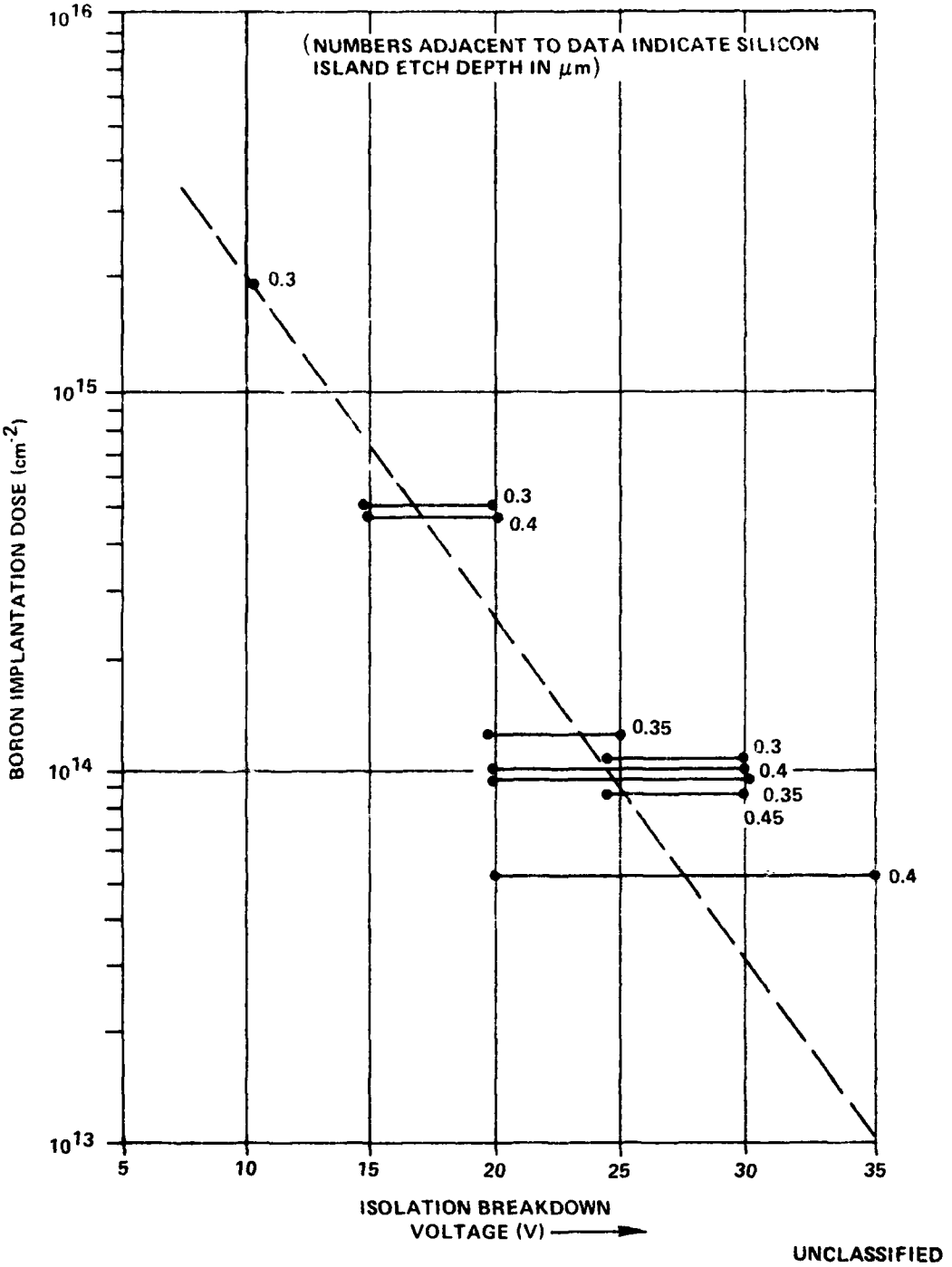


Figure 20. Isolation Breakdown Voltage versus Boron Implant Dose for Coplanar Isolation Experiments

4.3 Multipliers

The four-transistor multiplier cell can be drawn schematically as a bridge as shown in Figure 21. Three types of test patterns consisting of this multiplier cell were included on the test chip. One is a single stage multiplier with very large transistors (W = 2 mil, L = 2 mil). The purpose of this structure was to verify the basic theoretical advantages claimed for the four-transistor multiplier compared to the two-transistor multipliers used in previous attempts at making analog-analog correlators and to show the performance of such a multiplier when manufactured with relatively small geometrical errors.

The other two patterns used the fine geometry which would be used in a complete correlator and were designed to give information about inter- and intracell variations. One of these test patterns consists of an array of six multiplier cells as they would appear in the actual correlator, that is, with common output and individual inputs. The other pattern contains an array of ten multiplier cells with common inputs and separate outputs.

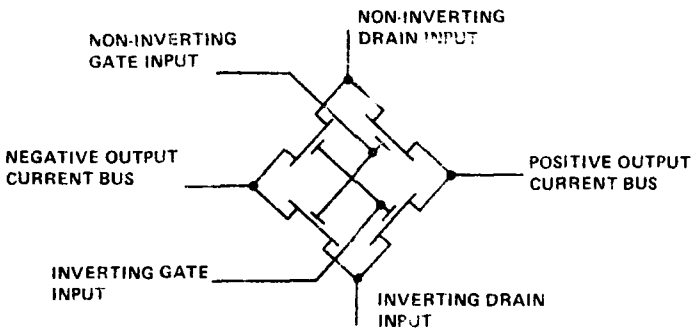


Figure 21. Schematic of the Four-Transistor Bridge Multiplier Cell

The multiplier cells are tested by applying two pairs of sinusoidal input signals. Each pair has a common dc component and opposite phase ac components. The pair applied to the gate inputs is at one frequency, f_G, while the pair applied to the drain inputs is at a different frequency, f_D. The two output current buses are held at a common dc bias, and the differential current is detected and displayed on a spectrum analyzer. The desired product output appears as two equal-strength sidebands at the sum and difference frequencies $|f_G|+|f_D|$ and $|f_G|-|f_D|$.

Spurious components at frequencies given by $|mf_G \pm nf_D|$, with integers m and n not both equal to one, will be generated both by the distortions inherent in the ideal field-effect transistor and by deviations from ideal behavior due to such factors as parameter variations and contact and interconnect impedances.

The performance of the four-transistor multiplier cell can be compared directly with that of the two-transistor cell simply by disconnecting one of the drain input signals. With that node floating, no current flows in that half of the bridge (the output buses are always at the same potential). Either half of the bridge can thus serve as a two-transistor multiplier. The gates can continue to be driven differentially, or one can be held at a dc level as would be the case when single-channel (nondifferential) CCDs are used.

4.3.1 Results for Large-Geometry Multiplier

Table 9 lists the results of a test with one of the large-geometry multipliers on Wafer 12, a wafer from the second phase of fabrication runs (see Subsection 4.1). With the exception of the entries for the desired product terms at the bottom of the table, which are expressed as dBV, all levels are expressed in dB relative to the product terms for the particular mode of operation. The relative noise level is the spectrum analyzer noise floor at the bandwidth selected for the measurement; it is not an indication of the multiplier's dynamic range. Blank entries in the table indicate that the particular frequency component was not visible above the noise floor. The input signals in this test were each at - 3 dBV (2 V peak-to-peak). The gate signals were at 5 kHz and drain signals were at 0.75 kHz.

TABLE 9. TEST RESULTS

Frequency (kHz)	Term	Relative Amplitudes (dB) Two-FET Cell with single-ended input	Two-FET Cell with differential inputs	Four-FET Cell with dual differential inputs
0.75	f_D	-10 dB*	-35 dB*	-41 dB*
1.50	$2 f_D$	-22	-41	-52
2.25	$3 f_D$	-25	-45	-54
2.75	$f_G - 3 f_D$			
3.00	$4 f_D$	-30		-41
3.50	$f_G - 2 f_D$	-12	-12	-42
5.00	f_G	-5	-6	-37
6.50	$f_G + 2 f_D$	-12	-12	-42
7.25	$f_G + 3 f_D$			-41
7.75	$2 f_G - 3 f_D$	-30		
8.50	$2 f_G - 2 f_D$	-29		
9.25	$2 f_G - f_D$	-15	-37	-49
10.00	$2 f_G$	-21	-41	
Noise Floor		-44	-50	-56
Product Output Level		-30 dBV	-24 dBV	-18 dBV

*Relative to product level

The amplitude of MOS multiplier outputs should be proportional to the product of the input levels with a proportionality factor as shown in Equation 5:

$$G = N\left(\frac{W}{L}\right) \mu RC$$

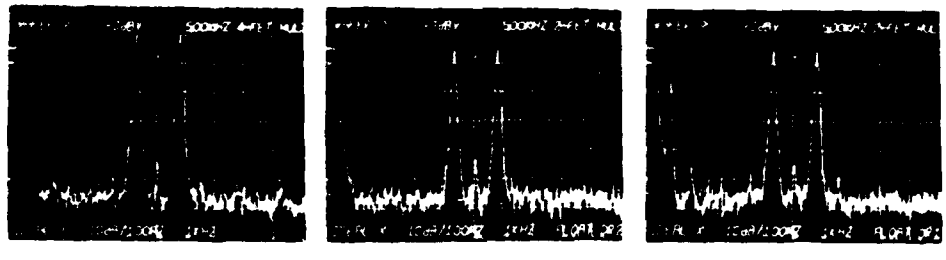
where W and L are the FET channel width and length; μ is the field effect mobility; R is the sensing resistance in the current detector (18 kΩ in our apparatus); and C is the oxide capacitance per unit area. The coefficient N is the number of transistors actively contributing to the generation of the product term. This is four for the bridge multiplier and two for the two-FET multiplier with differential gate inputs. When there is only a single gate signal input, the second transistor acts as a dummy transistor: consequently N = 1. The change in the value of N accounts for the 6 dB jumps in output level in Table 9. In some cases the absolute levels of spurious components were nearly the same in the different multiplier configurations. The relative level drops significantly in the bridge multiplier because of the greater amplitude of the desired output term.

For N = 4, (W/L) = 1, μ = 500 cm^2/V sec, R = 18 kΩ, and an oxide thickness of 1300 Å, we find that G has the value unity. For two input signals of -3 dBV, the output should be - 6 dBV, but since the power in each sideband is half, the spectrum analyzer would show -9 dBV.

The actual output was significantly lower. The discrepancy was traced to a problem with the contacts to the sources and drains. These contacts appeared to have in series a parallel combination of reversed diodes; that is, there was significant series impedance at low source-drain voltages, the precise condition under which the transistors are operated in a multiplier. Consequently, each transistor acted as a very poor multiplier, as confirmed by the first column in the table. Since four such poor multipliers were assembled into a bridge multiplier, however, the resulting circuit acted as a very good multiplier. This substantiated the theoretical observation that the bridge multiplier is a good multiplier by virtue of its symmetry alone, even when the four individual multiplying elements have high distortion.

Because the individual transistors on Wafer 12 were poor, the range of dc bias conditions over which the multiplier would perform well was limited. However, 200 mV variations in gate and drain levels had virtually no effect.

Wafer 9 was not as good as Wafer 12 from the standpoint of gate and junction breakdown, but its contacts were far superior. Correspondingly, the multiplier showed excellent response as illustrated by the series of photos in Figure 22. The product output level in Figure 22a is -13 dBV, only 4 dB less than the calculated value. All spurious signals are down by at least 50 dB except for feedthrough of the drain signal at a relative level of -18 dB. The two-transistor configuration of Figure 22b shows that excellent performance can be obtained with a two-FET multiplier under favorable conditions. Figure 22c indicates that the large drain signal feedthrough is associated with one side of the bridge only and is due to a defect in one transistor.



(a) SPECTRAL RESPONSE OF THE BRIDGE MULTIPLIER

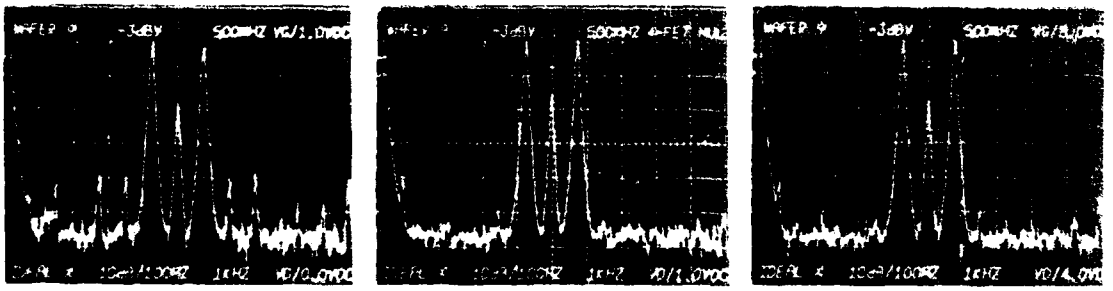
(b) RESPONSE OF FIRST HALF OF TWO-TRANSISTOR MULTIPLIERS WITH DIFFERENTIAL GATE INPUTS

(c) RESPONSE OF SECOND HALF OF TWO-TRANSISTOR MULTIPLIERS WITH DIFFERENTIAL GATE INPUTS

Figure 22. Multiplier Spectral Response

Despite such defects, the results with Wafer 9 showed spectacularly the ability of the bridge multiplier to perform well even with enormous bias variations. The series of photos in Figure 23 show the spectral response of the bridge multiplier over a range of bias conditions. In all cases the substrate was at -4 V and the current detection buses were held at ground. The substrate bias could be varied over a very wide range with no effect. It should be noted that the gate and drain signal frequencies had been interchanged so that the drain signal leakage due to the defective transistor were at 4 kHz.

Figure 23a was taken with the gate bias reduced to just above threshold (clipping of the negative signal excursions is occurring). Figure 23b shows the result with a drain bias offset of 1 V (the gate bias was about 4 V), and Figure 23c shows the extreme case of a 4 V drain offset at an 8 V gate bias. Figure 24 shows how the two-transistor multiplier responded under the conditions of Figure 23b. The drain offset caused a spurious feedthrough of the gate signal that was 6 dB larger than the product output! Drain offsets of only tens of millivolts resulted in significant multiplier error.



(a) (b) (c)

Figure 23. Spectral Response of Four-Transistor Multiplier Over a Range of dc Levels for Gate and Drain Signals

Figure 24. Spectral Response of Two-Transistor Multiplier with a One-Volt Offset in Drain Signals

4.3.2 Fine-Geometry Multipliers

Figure 25 shows a set of the spectra for all ten multipliers in one test pattern. The results were very uniform from circuit to circuit, and, with the exception of the feedthrough of the drain input signal at 4.5 kHz, all error signals were 50 dB down or lower.

The feedthrough of the drain input signal can result from variations in threshold voltage and/or transconductance. Transconductance variations, however, should result in some signal also at the second harmonic of the drain signal. Experimental results showed this term as much as 32 dB lower. It, therefore, appears more likely that a threshold voltage difference was responsible for the feedthrough.

Moreover, the term was not entirely the result of random variations. Figure 26 shows spectra for three of the multipliers each operated in the two possible ways as a two-FET multiplier. The feedthrough error was always greater when one of the drain signals was disconnected. We concluded that some subtlety of the mask layout resulted in a systematic difference among the four transistors.

The spectra in Figure 26 also show the larger error terms of the two-FET multiplier, the main ones being at f_G and $2\ f_D \pm f_G$. If the multipliers had been operating with a nondifferential gate signal, the desired output terms would have been 6 dB lower and the error terms even larger.

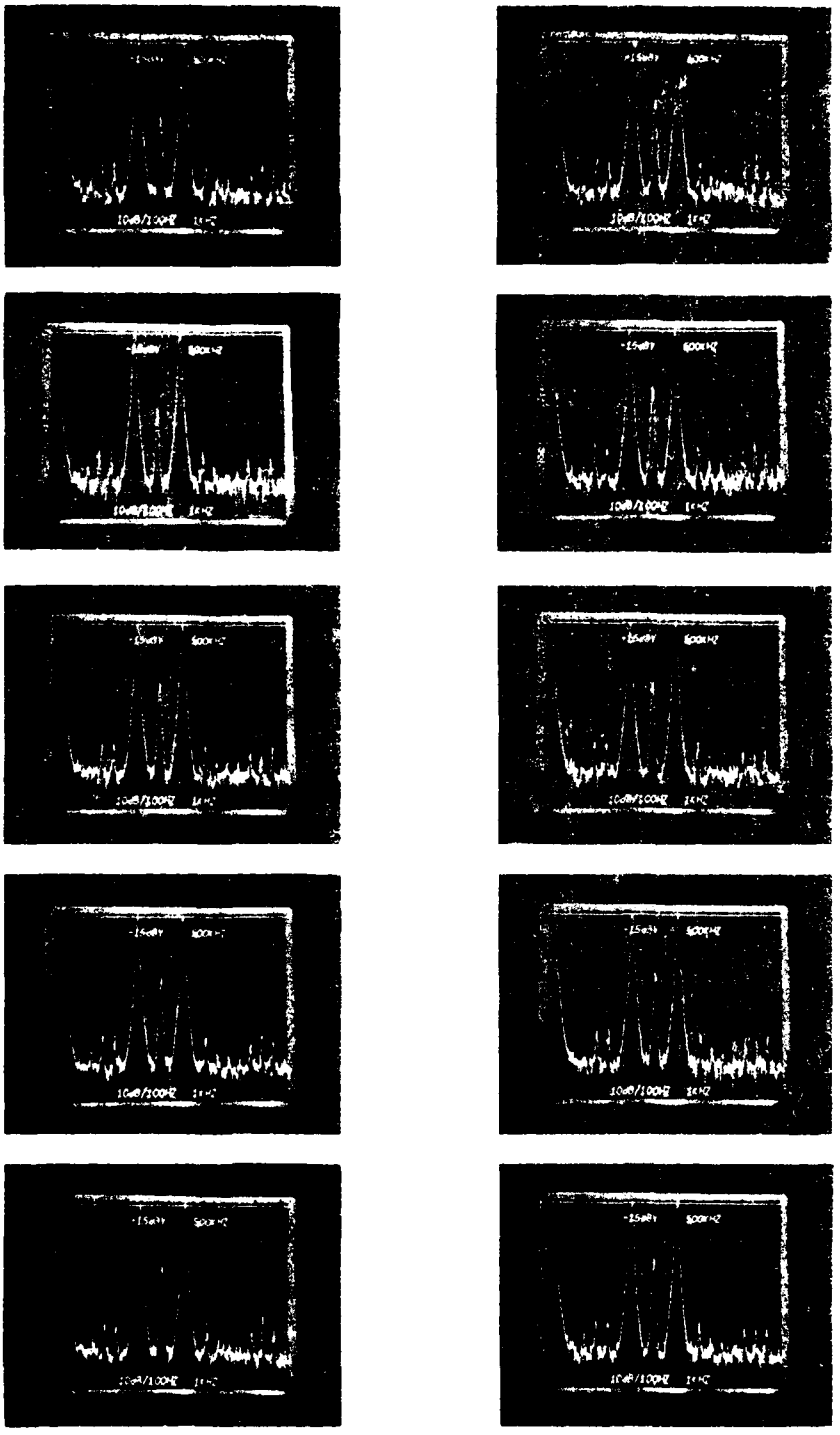


Figure 25. Output Spectra of Multiplier Test Patterns

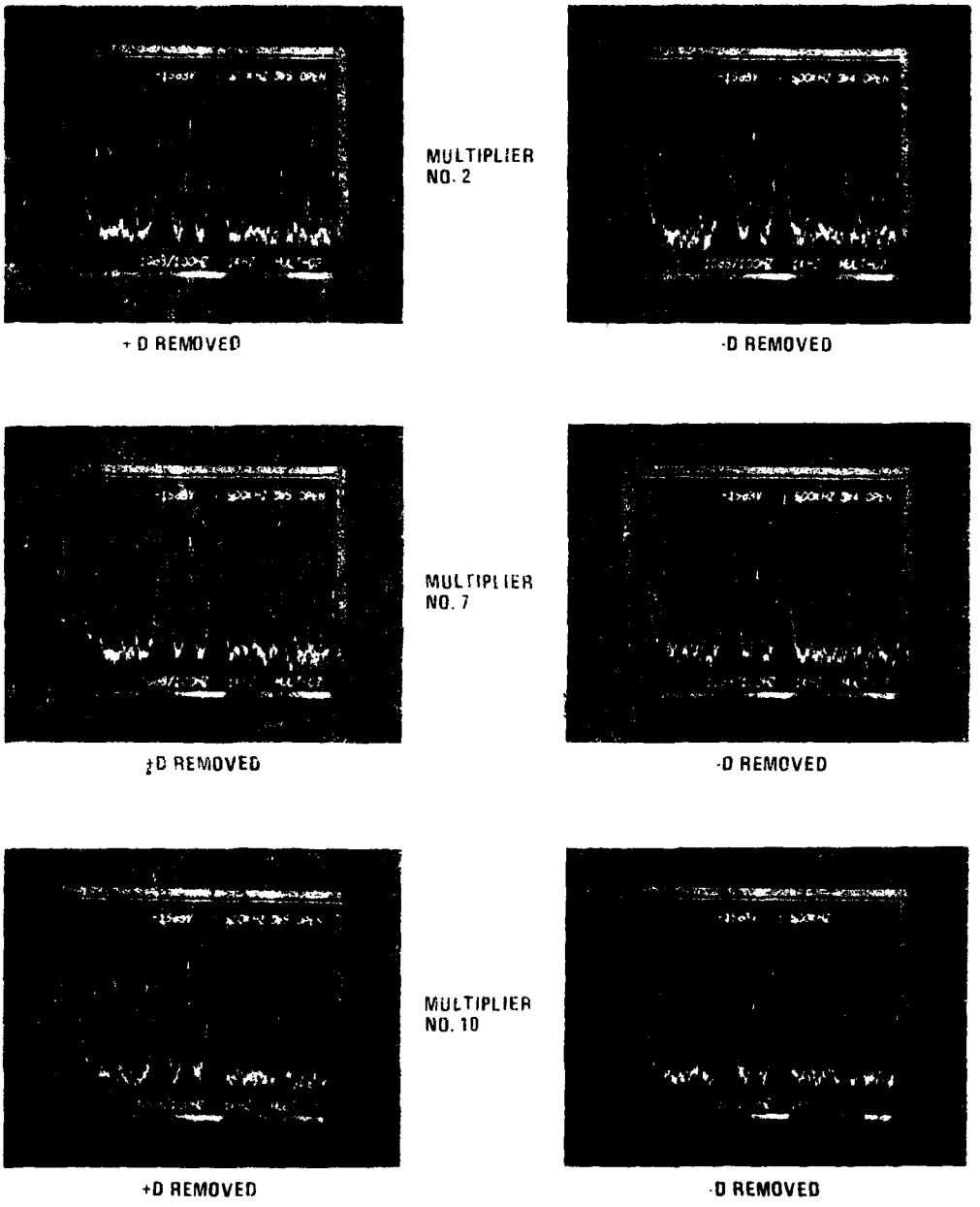


Figure 26. Response of Bridge Multipliers Operated as Two-FET Multipliers

4.4 Source Followers

The dc offset characteristics of the source followers on the CCD test pattern were investigated by turning the float-control gates ϕ_c on with a 15 V bias and using ϕ_3 to set the floating gates to a fixed dc level. This test configuration is shown in Figure 27. The output voltages V_{out} were measured for the four outer and four inner taps on numerous test patterns. Some typical results are shown in Table 10.

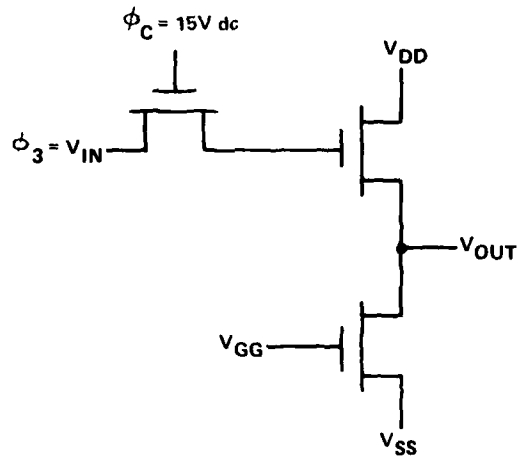


Figure 27. Source Follower Circuit

There are a number of useful statistics to be examined for the entire set of test data. For example, one can look at how uniform the outputs are for a set of four contiguous source followers. The smallest standard deviation was 5 mV, the largest, 29 mV, and the mean standard deviation, 15 mV.

Next, one can look at the mean output voltage from one test pattern to the next. Comparing outer sets of source followers only, we find a mean of 3.254 V with a standard deviation of 70 mV. Similarly, comparing inner

TABLE 10. OUTPUT VOLTAGE TEST RESULTS

		Pattern 1	Pattern 2	Pattern 3
	1	3.219	3.219	3.417
Outer	2	3.208	3.237	3.398
Outputs	3	3.219	3.225	3.394
	4	3.220	3.272	3.406
Mean		3.217	3.238	3.404
Standard Deviation		0.006	0.024	0.010
	1	3.102	3.151	3.232
Inner	2	3.141	3.156	3.239
Outputs	3	3.164	3.173	3.253
	4	3.136	3.157	3.245
Mean		3.136	3.159	3.242
Standard Deviation		0.026	0.010	0.009

sets of followers, we find a mean of 3.192 V with a standard deviation of 50 mV. The systematic difference between outer and inner followers that is apparent in the data in Table 10 is borne out by the full set of data, where there is a 60 mV average difference between outputs. Since the source followers on the two sides of the CCDs are separately biased, this systematic difference can be partially compensated for. The implications to be drawn from the data of Table 10 will be discussed further in Section 5.

4.5 Complete Correlator

A preliminary attempt was made to operate the 32-stage correlator test pattern and succeeded on the first try. Clock waveforms were generated with operational amplifiers, whose slow slewing limited the clock frequency to about 5 kHz. An operational-amplifier-gated current integrator was used to look at the output charge from each of the four CCDs. There was no discernible charge transfer loss in traversing the 32 stages, and the delay of about 6 ms from the input to the output was consistent with the 5 kHz clock frequency.

The upper trace in Figure 28 shows the output of the correlator when operated with the same signal applied to both the signal and reference channels and clocked through together. The lower trace shows one of the input signals. As the pulse enters the CCD, the output grows linearly until the entire length of the CCD is filled. Then the output level remains constant until the input pulse ends, after which a 6 ms linear ramp returns the signal to its original level.

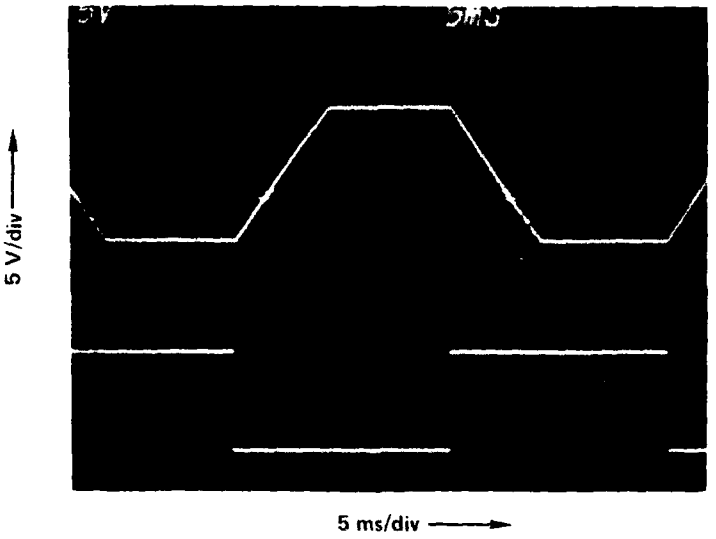


Figure 28. Complete Correlator Response

This test did not represent a full check of the operation of the correlator. It did, however, verify the functionality of each element of the chip: CCDs, floating gates, float-control switching FETs, source follower buffers, multipliers, and summing busses.

4.6 Automated Testing

The results described thus far were obtained using manually operated laboratory test equipment. By necessity, the data shown represents only a limited number of test attempts. However, since the distributions of circuit operation parameters were expected to be one of the factors limiting the performance of the correlator/convolver, the use of automated test equipment for the gathering and processing of the data from the test patterns was planned for this program at an early stage. The progress made performing this work is described below.

As described in previous sections of this report, an error analysis of the correlator/convolver was performed. This analysis showed that, by virtue of symmetry and close location, the multiplier transistors will not be the major source of such errors. The major source is expected to be the lack of perfect matching of the offset voltages associated with each pair of source followers driving the multipliers. If, for example, we assume that a 2 V peak-to-peak input is achieved at the multiplier input nodes, each pair of source followers delivering the inputs must have a match of its two quiescent output levels to within 20 mV. This maximum mismatch of 20 mV includes all errors and must be maintained in spite of the relatively large spacing between the two source followers (appriximately 40 mils). The offset error will have first order contributions from variations in threshold and transconductance of the source follower drivers, floating gate reset clock feedthrough capacitance, and interconnect IR drops. Variations of transconductance and threshold of the source follower load devices are expected to have only second order effects.

While the computer analysis of the performance of the circuits in the correlator/convolver showed how much source follower offset voltage mismatch could be tolerated, it could not provide an indication of what parameter variations were actually being obtained in the test structures or provide the feedback needed for process improvement in the future.

With the above in mind, four software programs were written, debugged, and used to investigate parameter variations on several wafers of correlator/convolver test patterns using the MITE and Sentry 7 test systems as shown in Table 11.

TABLE 11. CORRELATOR/CONVOLVER TEST PATTERN AUTOMATED TEST PROGRAMS

Tester	Program
Sentry 7	Threshold and transconductance variations of the transistor test patterns (five different geometries in clusters of 5 devices).
MITE	Same as above.
MITE	Output voltage level variations for the floating gate tap source followers in the differential CCD test patterns.
MITE	Transconductance and threshold variations of the CISO (Common Input Separate Output) multiplier test pattern transistors.

All test data were taken at microamp current levels comparable to the final operating conditions. Unfortunately, the measurement capability of both systems proved to be marginal for the tasks to be performed. In addition, Sentry 7 could only provide parameter distributions for the entire wafer. It could not compile distributions of matches of parameters within a chip without extensive new software.

Table 12 lists the performance specifications of both testers in the measurement ranges used for the measurement of the correlator/convolver test patterns.

TABLE 12. SPECIFICATIONS OF SENTRY 7 AND MITE TEST SYSTEMS FOR g_m AND V_t MEASUREMENT AT LOW LEVELS

	Gate Voltage			Drain Current		
	Range	Resolution	Accuracy	Range	Resolution	Accuracy
Sentry 7	0-2 V	2 mV/step	0.1 percent ±2 mV	0-1 μA	1 na/step	±0.5 percent ±10 nA
MITE	0-1 V	1 mV/step	1 percent ±2 mV	0-10 μA	10 na/step	±1 percent ±100 nA

The above chart lists percent accuracies in percent of programmed value. Although the current range, resolution and accuracy are entirely adequate for devices operating at 10 to 20μA drain currents, the gate voltage

resolution and accuracy is marginal for the correlator/convolver since these are within an order of magnitude of the desired match of threshold voltage between nearby devices.

The software of Table 11 was developed in full recognition of this problem, assuming that measurements made within a short time of each other would probably reflect a better-than-specified accuracy.

The data from both automated testers was found to have less accuracy than expected because of quantization error. A considerable amount of data was collected, and in spite of the marginal accuracy of some of the measurements some useful information was obtained. Figures 29 through 33 show sections of several wafer maps prepared from data taken using the Sentry 7 and MITE systems to determine the distributions of threshold variations within five-transistor clusters across wafer 16. Five different transistor types were measured. Each wafer map shows the mean and standard deviation of Vt at six test pattern locations using a source-drain voltage of 10 V and drain currents of 1 and 10 μA.

The standard deviations of Figures 29 through 33 are plotted in Figure 34 in a channel length (L) by channel width (W) format. In view of the way the standard deviations vary with drain current, one cannot conclude that there is any clearly statistically significant difference between the values. Halving the channel width from 0.4 to 0.2 mils does not appear to cause a large increase in threshold voltage variation. The use of a very short channel length (0.35 mils) may result in some increase in parameter variation.

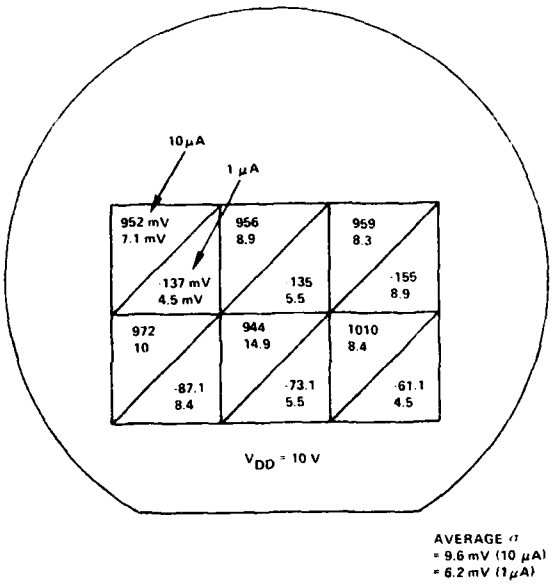


Figure 29. Threshold Means and Standard Deviations of Five 0.2 x 0.8 Mil (Channel Wand L) Multiplier Transistors (Wafer 16)

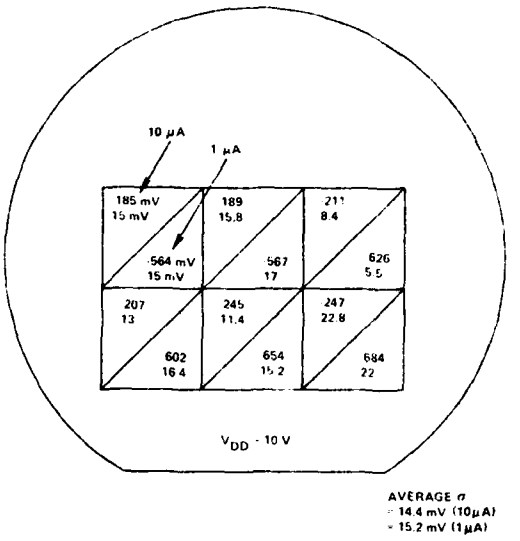


Figure 30. Threshold Means and Standard Deviations of Five 0.4 x 0.35 Mil (Channel W and L) Source Follower Driver Transistors (Wafer 16)

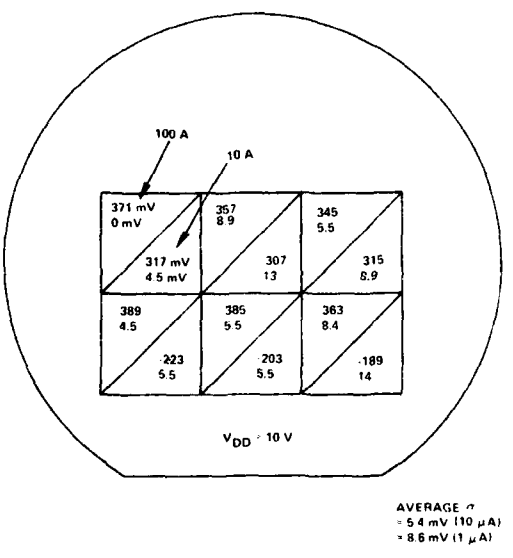


Figure 31. Threshold Means and Standard Deviations of Five 0.4 x 0.675 Mil (Channel W and L) Source Follower Drain Driver Load Transistors (Wafer 16)

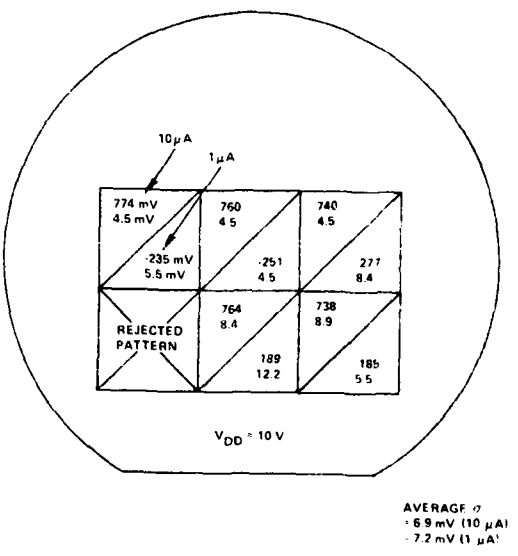


Figure 32. Threshold Means and Standard Deviations of Five 0.4 x 1.15 Mil (Channel W and L) Gate Driver SF Load Transistors (Wafer 16)

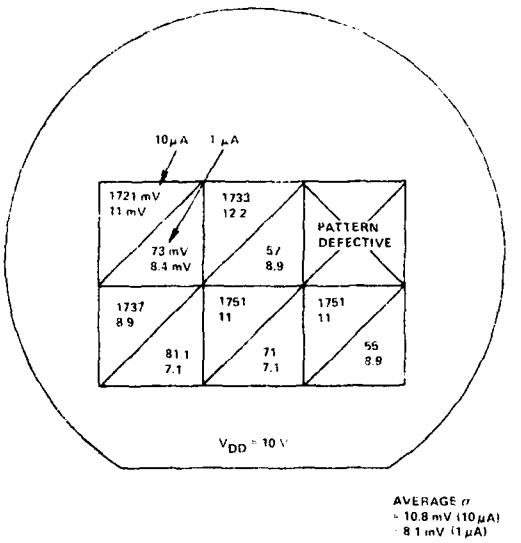


Figure 33. Threshold Means and Standard Deviations of Five 0.2 x 1.6 Mil (Channel W and L) Possible Multiplier Transistors (Wafer 16)

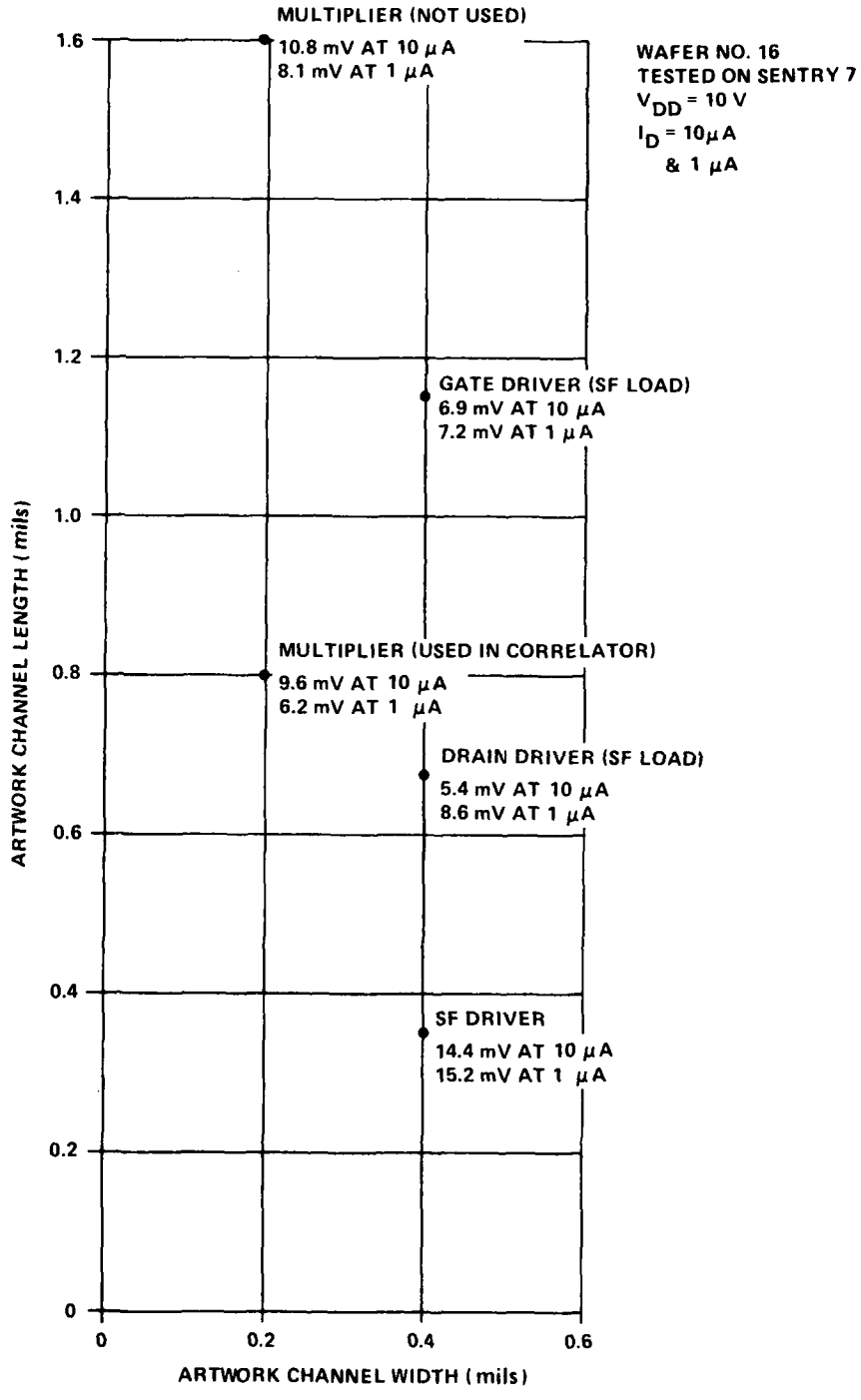


Figure 34. Average Standard Deviations of Threshold Voltage of Five Transistors of same Geometry from Six Adjacent Patterns Spaced 1.2 Mils Apart

SECTION V
CONCLUSIONS AND PLANS FOR THE NEXT REPORTING PERIOD

Four-transistor MOS bridge multipliers geometrically compatible with a complete correlator/convolver have been fabricated with performance that exceeds contract requirements. One problem has been encountered with some of the multipliers - an error term representing direct feedthrough of the drain input signal. This error is not random but systematic, a fact that gives us confidence that it can be corrected easily. There is some indication that the problem arises from the fact that one of the four transistors in the bridge has a second layer of polysilicon over the channel which acts as a barrier to hydrogen diffusion during the anneal process. Increasing the anneal time was found to reduce the problem. The final design of the correlator/convolver will relocate the upper poly line so that it does not cover the transistor channel.

The multiplier performance data, the manual measurements on source follower characteristics, and the automated testing of transistor clusters all show that short-range random variations in parameters such as threshold voltage and transconductance are small enough to meet contract requirements. In a 256-stage correlator/convolver there will in all likelihood be some stages whose inaccuracies exceed the 1 percent goal and others whose accuracy greatly exceeds the requirement. On the whole, short-range random parameter variations are consistent with the overall performance desired for the correlator/convolver.

Long-range random or systematic variations are not a problem by virtue of the characteristics of the bridge multiplier. Medium-range random variations, however, can be a problem and, at present, are larger than desired. Process experiments will be run during the next reporting period to determine methods to obtain more uniform thresholds and transconductances in devices in future correlator/convolvers. These experiments will concentrate primarily on the following:

1) Use of starting material with more uniform resistivity
2) Obtaining more uniform fixed charge (Q_{SS}) through annealling techniques
3) Achieving more uniformly doped polysilicon

In addition, some mask changes for improving device uniformity will be investigated. Especially helpful would be a change in the mask pattern generator software to permit a single aperture setting to be used to make all exposures of a given channel dimension. At present, the pattern generator makes exposures cell-by-cell, resetting the aperture many times between the exposures of identical areas. If polysilicon resistivity (and, thus, work-function) variations are identified as the source of medium-range variations, we can use titanium-tungsten-aluminum gates for critical transistors.

During the final reporting period, the 256-stage correlator/convolver will be designed incorporating the improvements suggested by data obtained from the current test structures.

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